A multi-layer research and training platform for system-on-chip testing:

Hardware, Software and Web Interface

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Outline

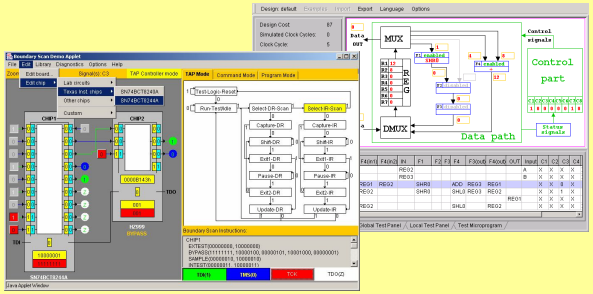
- ✓ Introduction and motivation
- ✓ Different layers of the platform
- ✓ HW tools
- ✓ PC-based tools
- ✓ Web interface
- ✓ E-Learning tools
- ✓ Conclusions and discussion

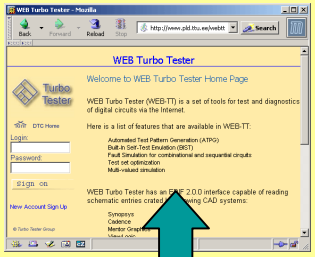
Motivation

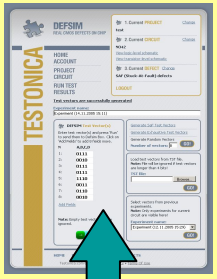
- ✓ Cutting Edge Research
  - Needs custom developed algorithms and/or tools
- ✓ PhD Students
  - Need to run their experiments
- ✓ Undergraduate Students
  - Need introduction to the topic
- ✓ Department
  - Needs training materials and research

Different layers of the platform

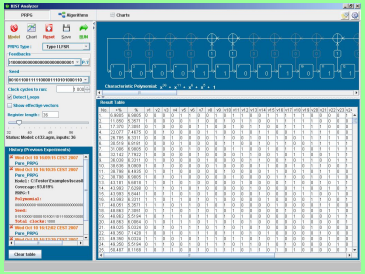
Web Tools

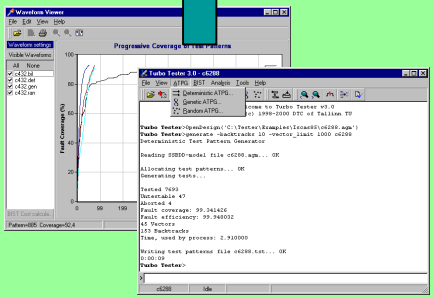


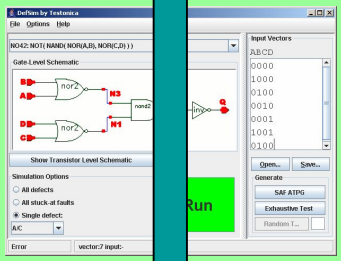




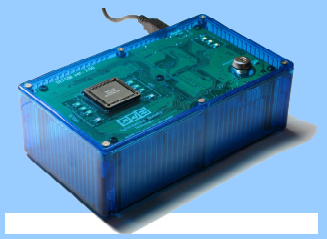
PC Tools





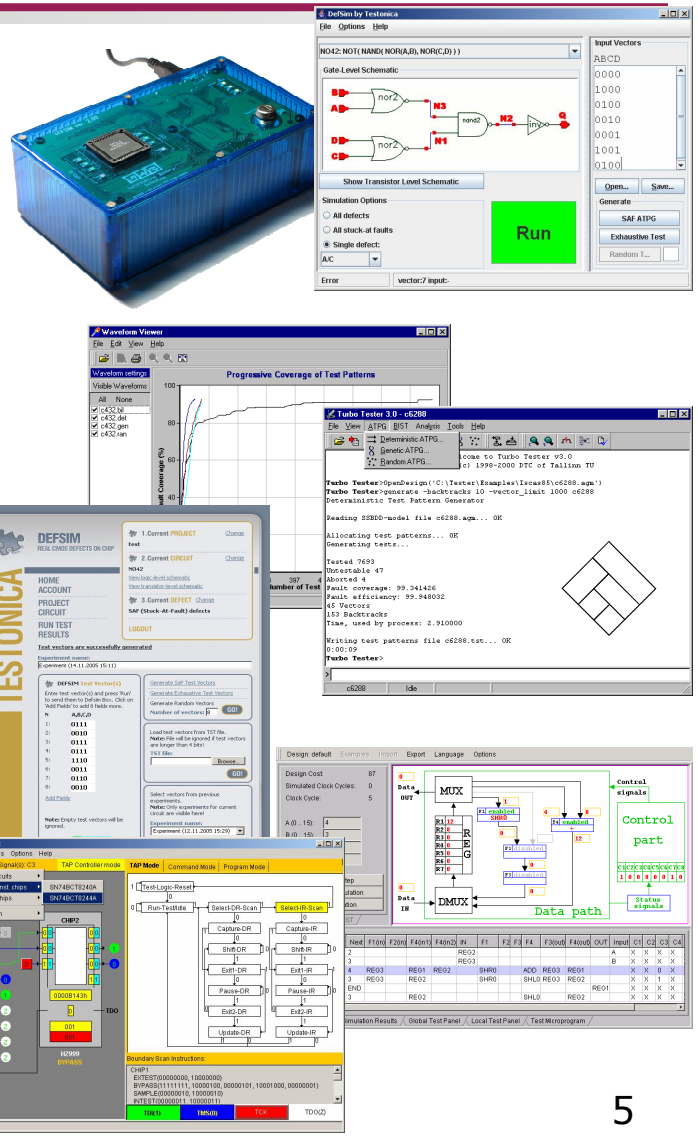


Hardware Tools



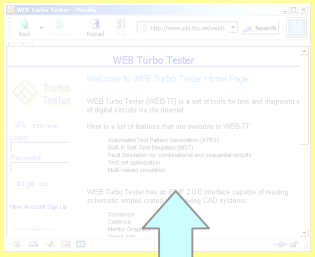
Main components of the platform

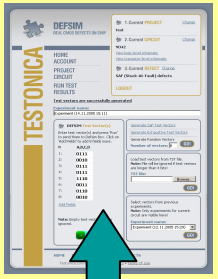
- ✓ DefSim - an integrated measurement environment for physical defect study in CMOS circuits.
- ✓ TurboTester – a research and training toolkit with extensive set of tools for digital test and design for testability
- ✓ Web-based runtime interface for remote access to our tools
- ✓ Java applets – illustrative e-learning software written specifically for the web
- ✓ Other tools



Different layers of the platform

Web Tools





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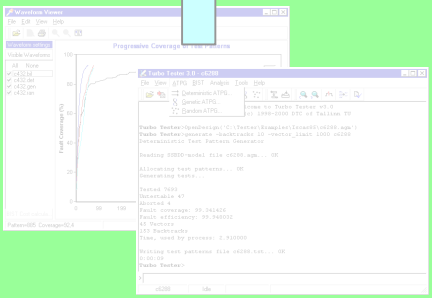

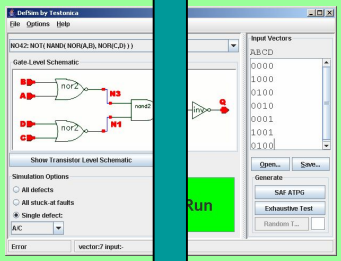

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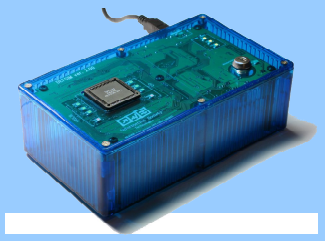
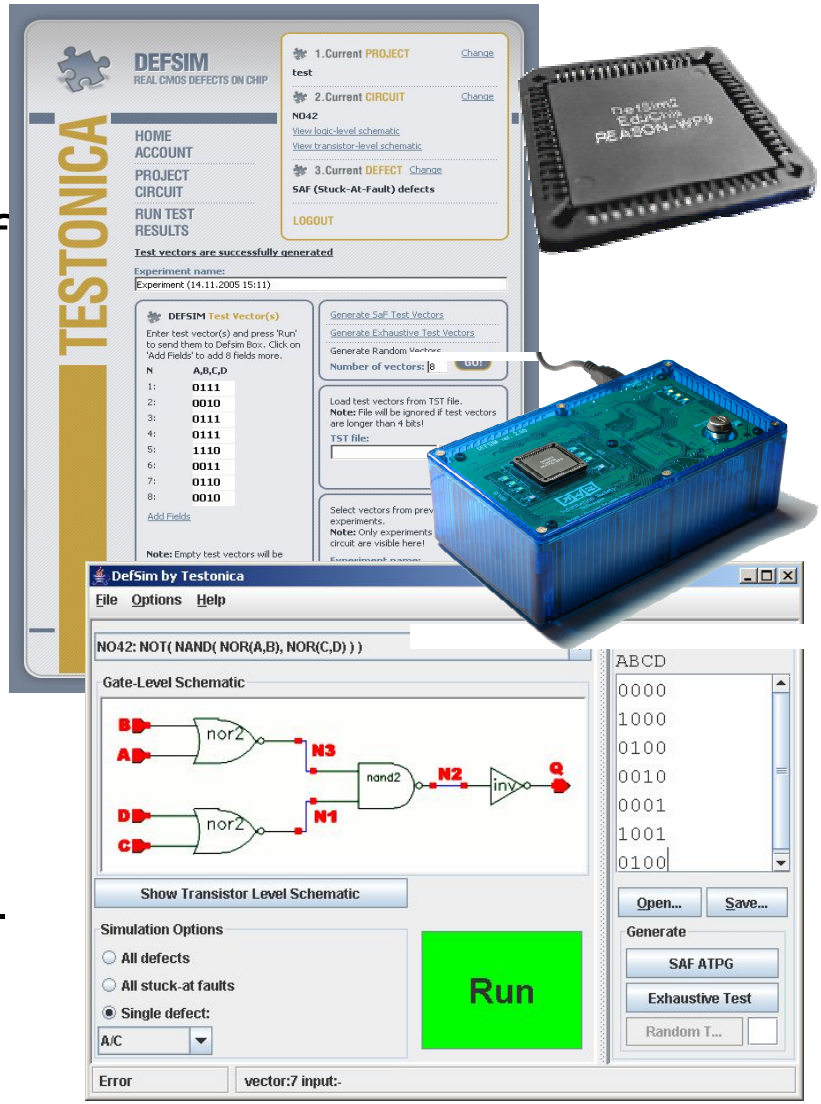


Defect Study using DefSim

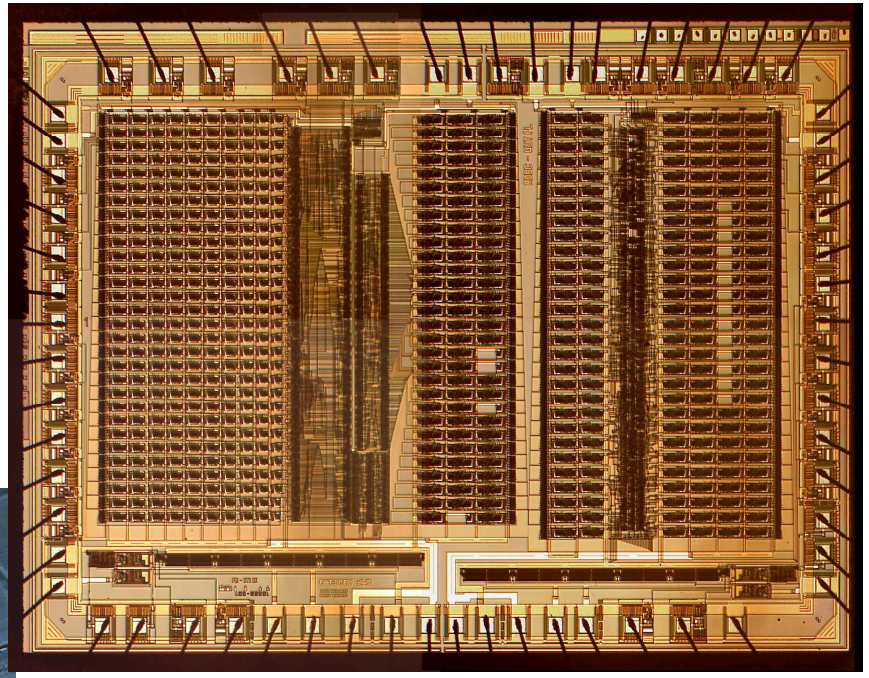
- DefSim is an integrated circuit (ASIC) and a measurement equipmrnt for experimental study of CMOS defects.
- The central element of the DefSim equipment is an educational IC with a large variety of shorts and opens physically inserted into a set of simple digital circuits.
- The IC is attached to a dedicated measurement box serving as an interface to the computer. The box supports two measurement modes - voltage and I_{DDQ} testing.

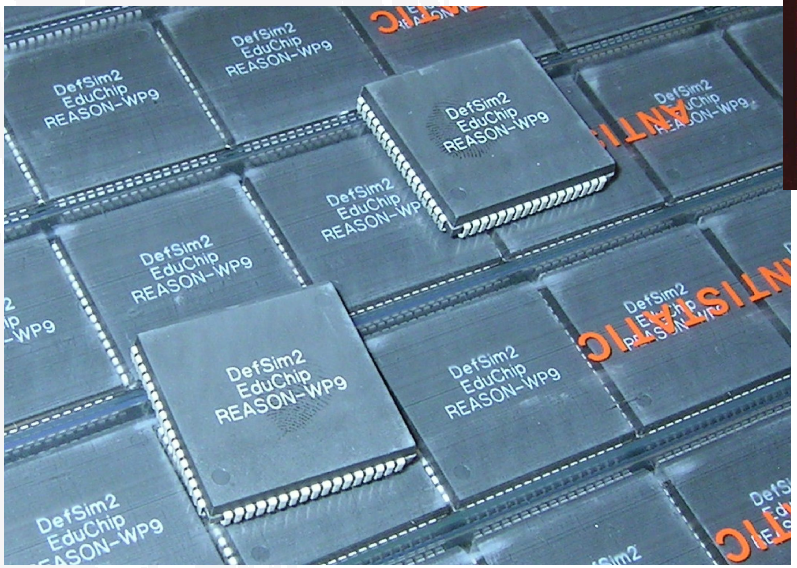


http://www.defsim.com

DefSim IC details

- Standard industrial CMOS technology
- Area 19.90 mm^2
- Approx. 48000 transistors
- 62 pins
- JLCC68 package

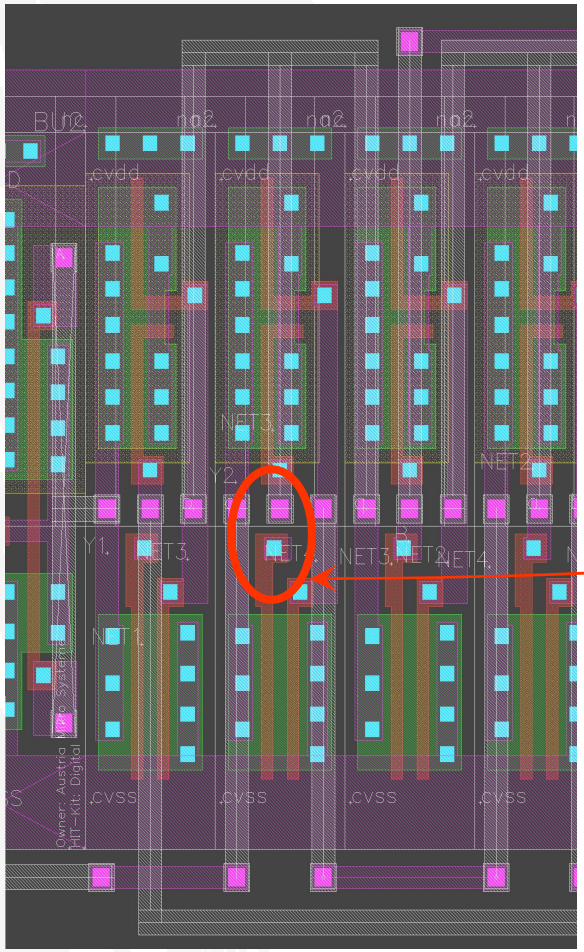


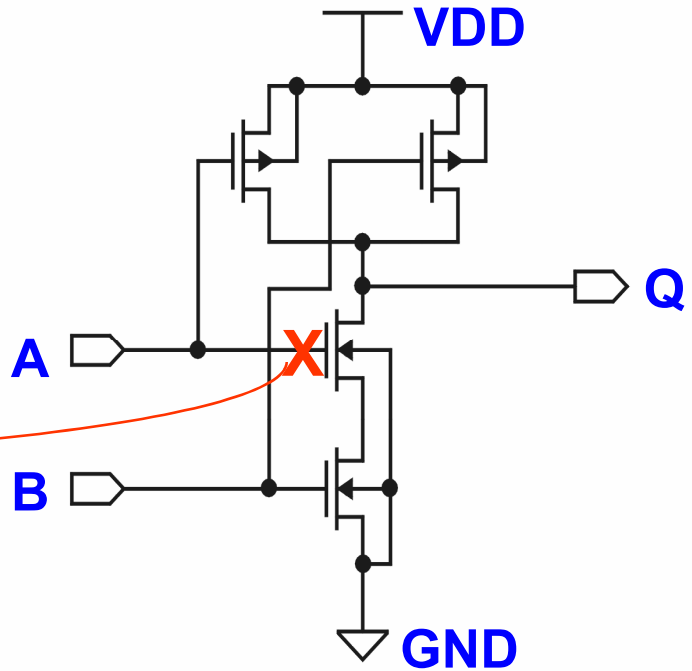


A built-in current monitor for I_{DDQ} *testing* is implemented in each block.

Implementation of defects

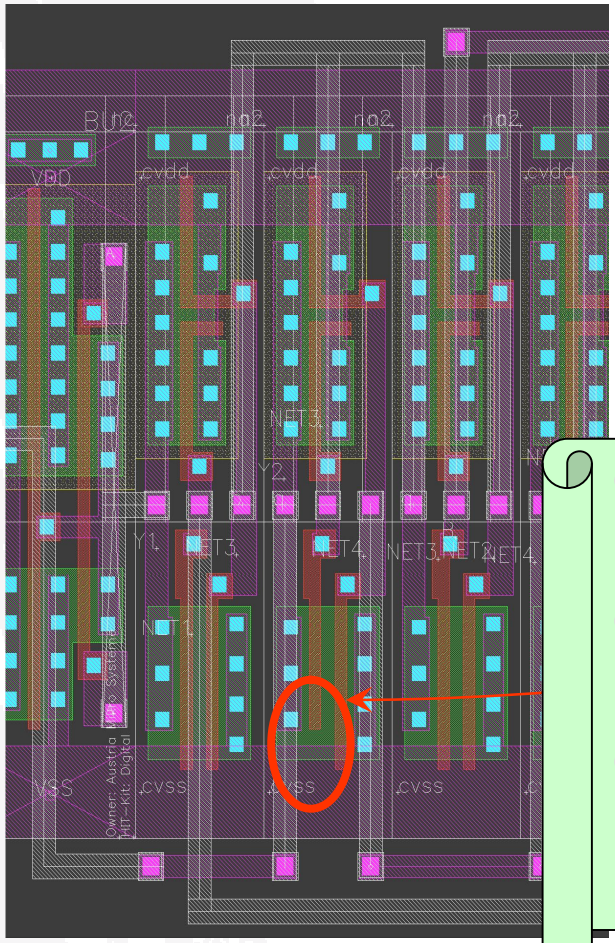
NAND2 cell with floating gate

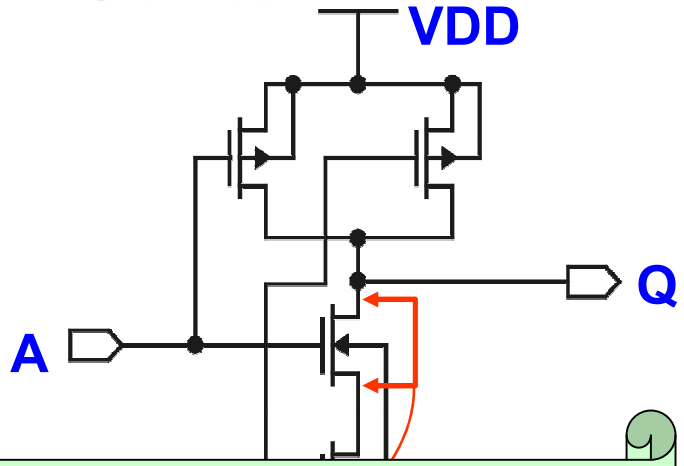




Implementation of defects

NAND2 cell with D-S short (missing poly)





- Altogether there are over 500 different defects on the chip
- Implemented defects are shorts and opens in metal and poly layers
- To be close to the silicon reality each cell is loaded and driven by standard non-inverting buffers

DefSim in the classroom

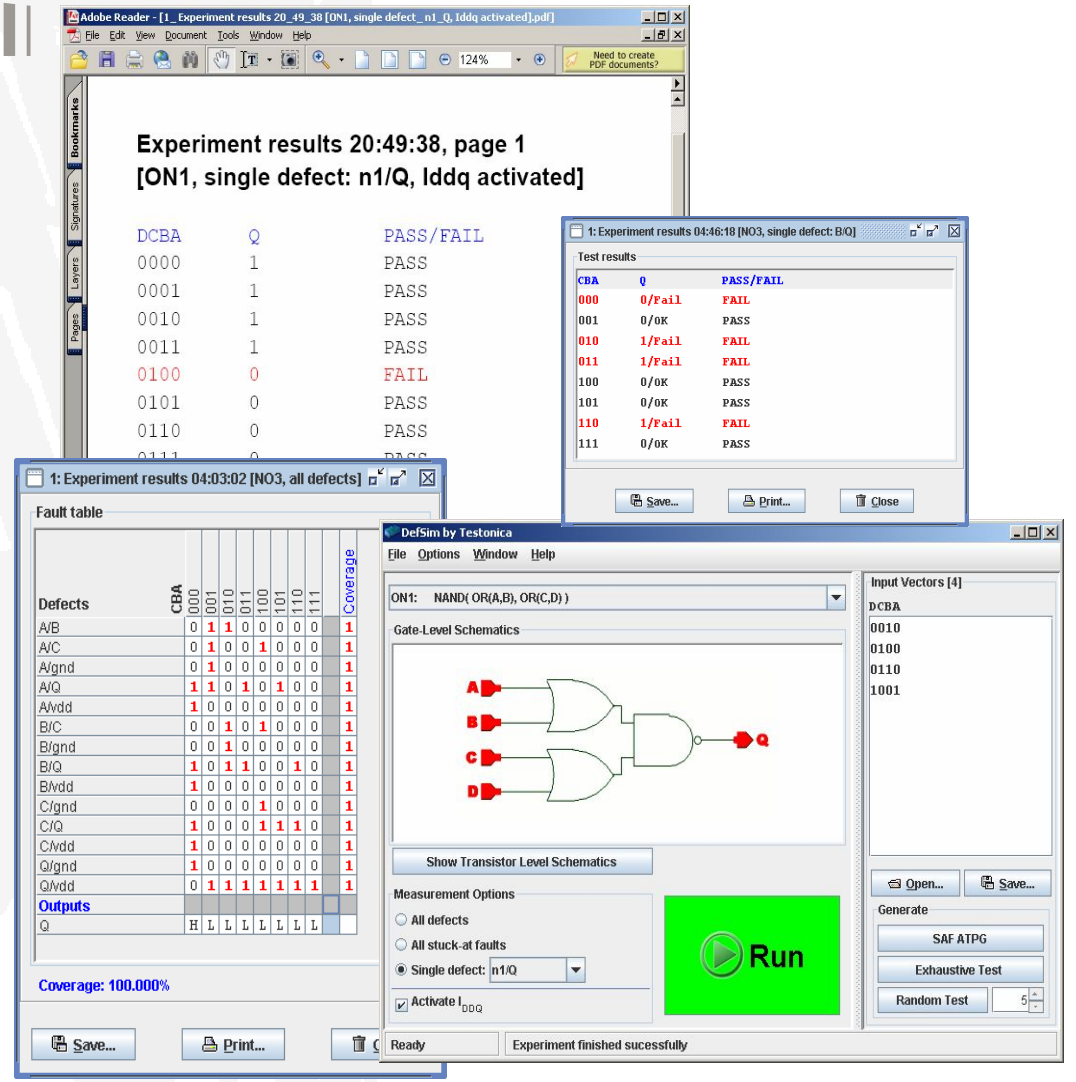
- ✓ *With DefSim you can*

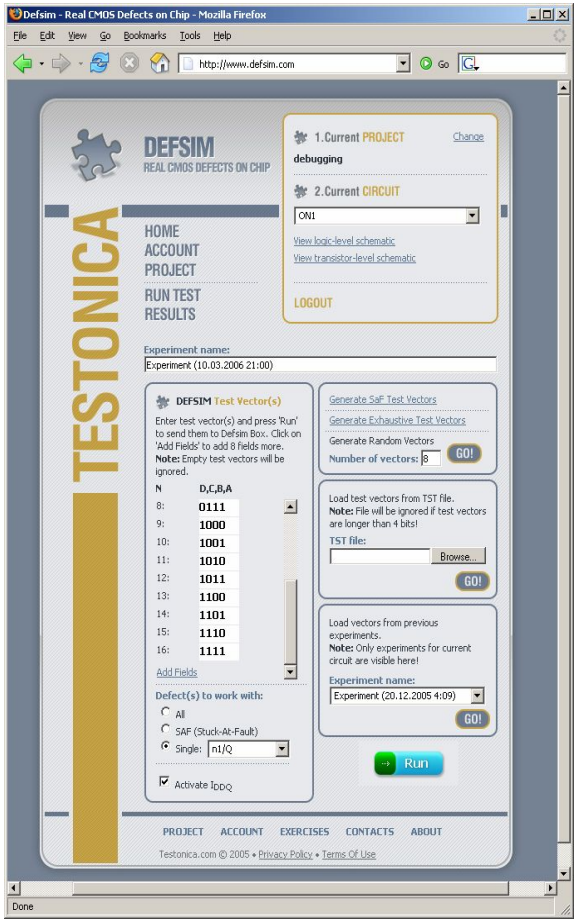
- ✓ Observe the truth table of correct circuit
- ✓ Observe the truth table of defective circuit
- ✓ Obtain defect/fault tables for all specific defects
- ✓ Define test patterns automatically or manually
- ✓ Activate IDDQ and voltage measurements
- ✓ Study behavior of bridging and open faults
- ✓ Study and compare different fault models

DefSim lab environment

"Plug and Play" – dedicated hardware and software

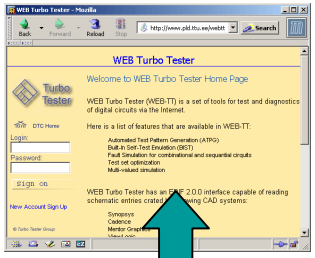
DefSim user interface

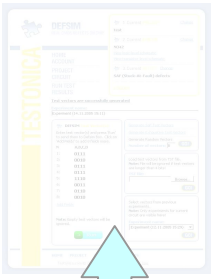




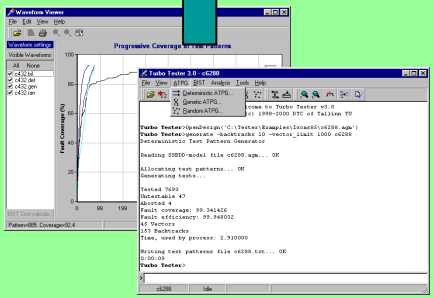
Different layers of the platform

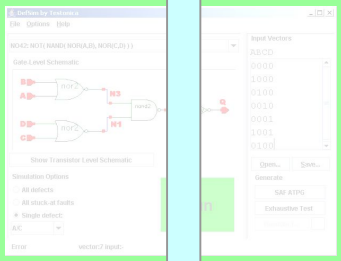
Web Tools





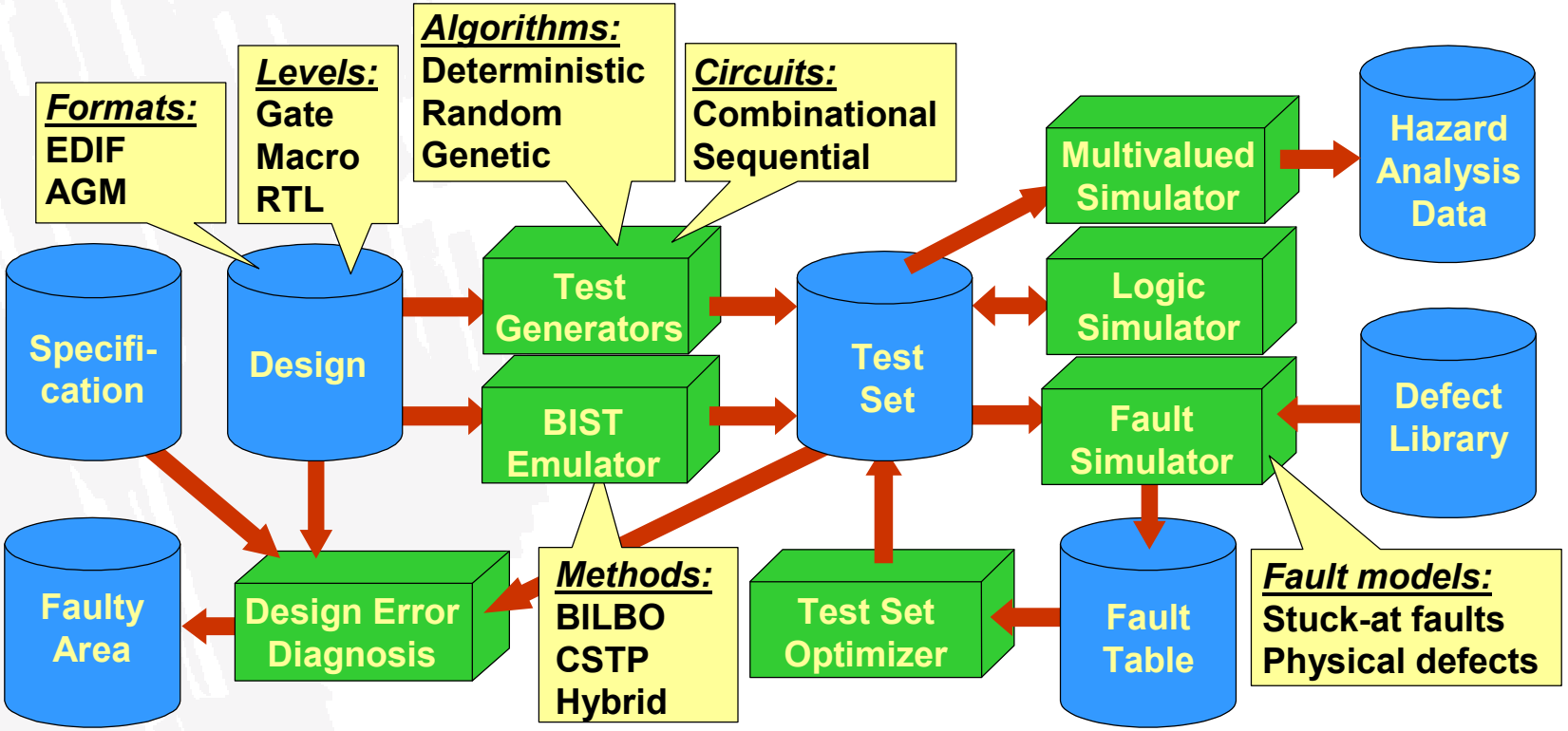
PC Tools





Hardware Tools

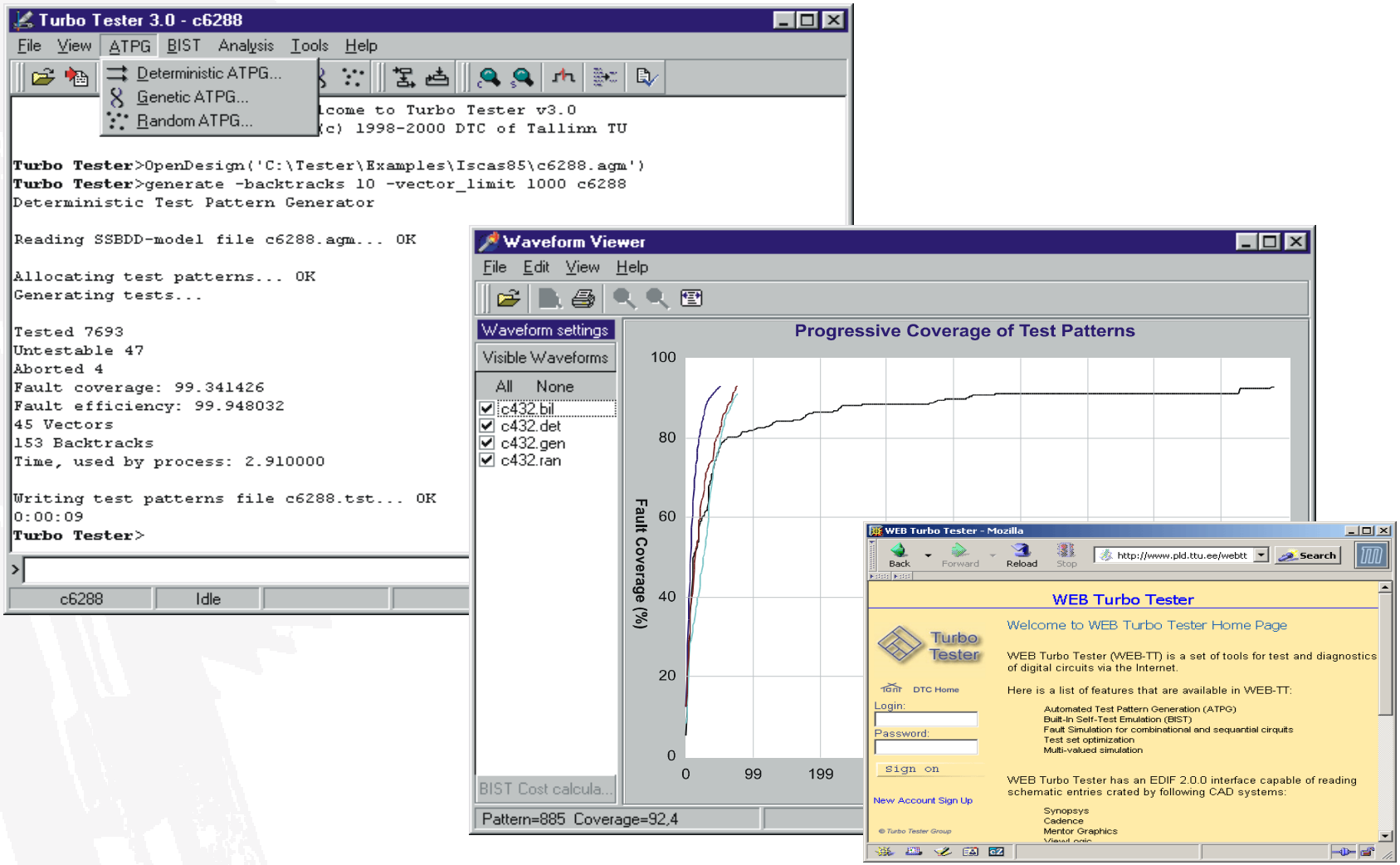
PC-Based Toolkit – Turbo Tester



http://www.pld.ttu.ee/tt

Used in 100+ institutions in 47 countries

Turbo Tester's user interface



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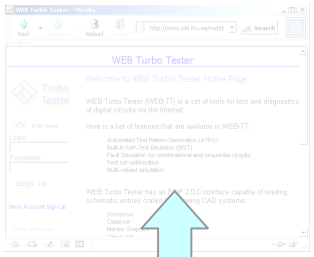
Turbo Tester: Basic Facts

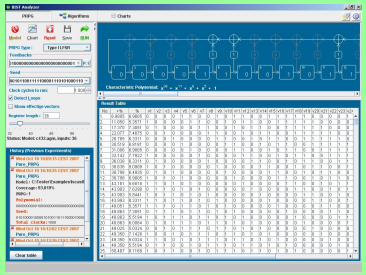
- ✓ Freeware
- ✓ Downloadable via the Web
- ✓ Windows, Linux, UNIX/Solaris
- ✓ EDIF design interface
- ✓ ATPGs, BIST, simulators, test compaction
- ✓ Provides homogeneous environment for research and training

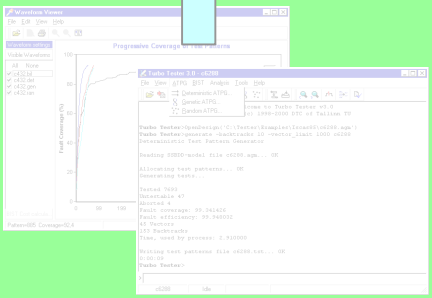
Different layers of the platform

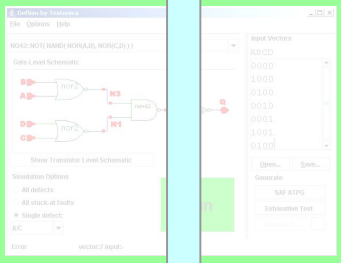
Web Tools



PC Tools





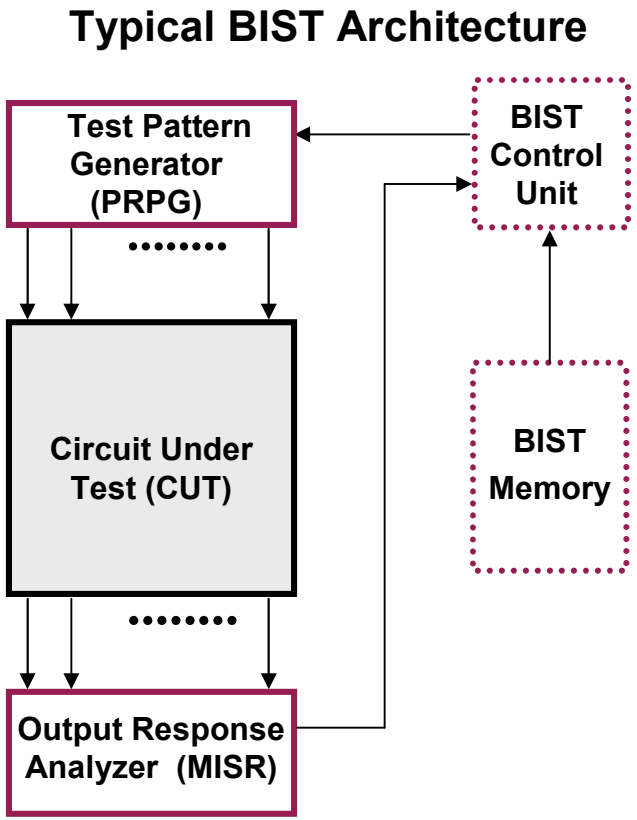


Hardware Tools

BIST Analyzer: covered topics

- ✓ Test Pattern Generators (PRPG):
  - LFSR
  - Modular LFSR
  - Cellular Automata
  - *GLFSR*
  - *Weighted TPG*
  - *etc.*

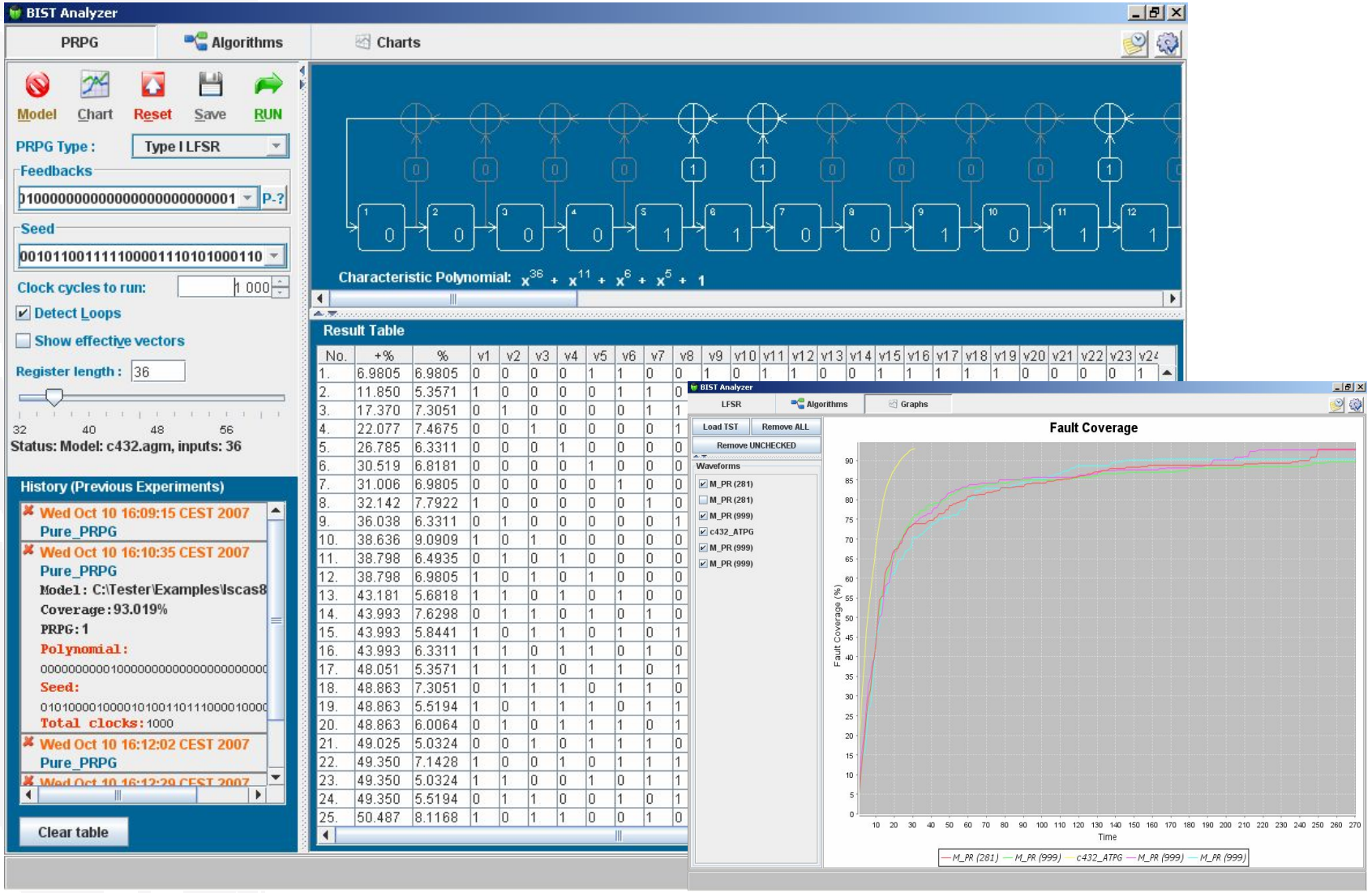
- ✓ Combined Techniques (PRPG + Memory):
  - Reseeding
  - Multiple polynomial BIST
  - Hybrid BIST
  - *Bit-Flipping BIST*
  - *Column matching BIST*
  - *etc.*



BIST Analyzer: covered topics

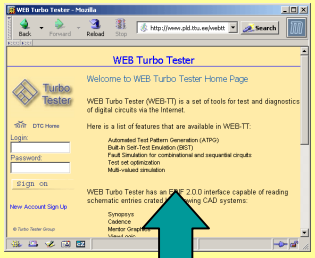
- Different embedded generators (PRPG) and their properties
- PRPG optimization methodologies and algorithms
- Mixed-mode BIST solutions (PRPG+memory)
- Fault detection and diagnosis in BIST

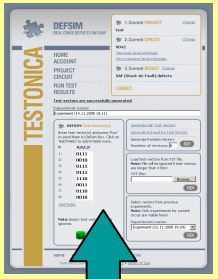
BIST Analyzer



Different layers of the platform

Web Tools





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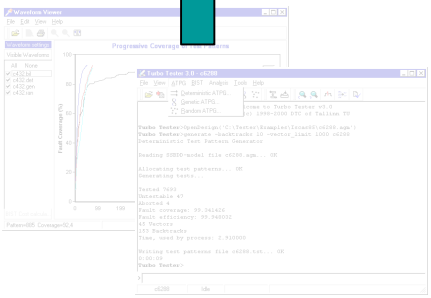
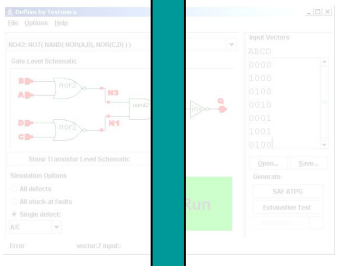
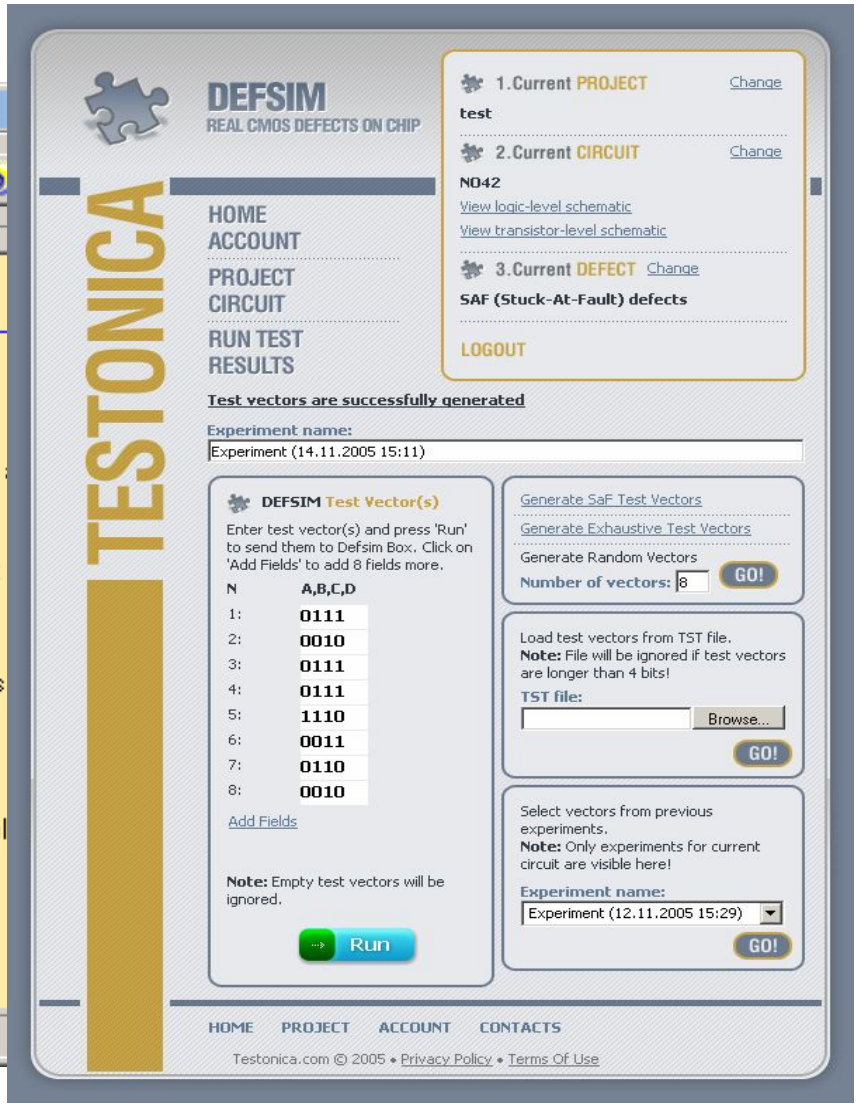




Hardware Tools

Web Interface



Different layers of the platform

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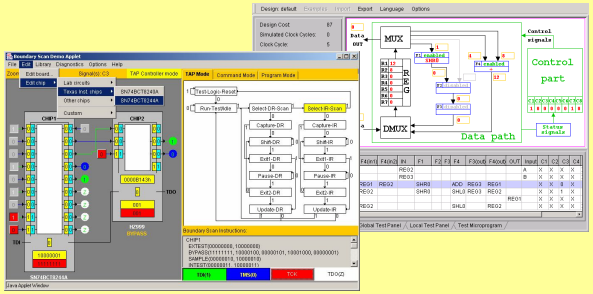

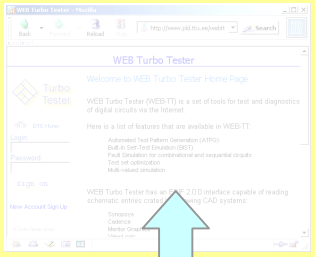

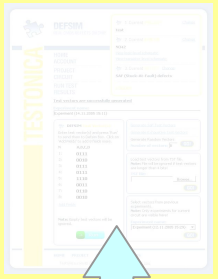

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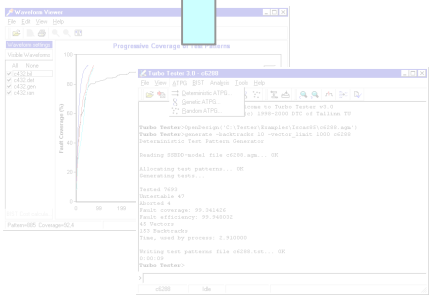
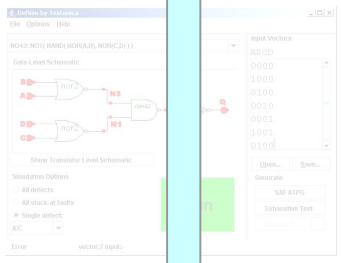
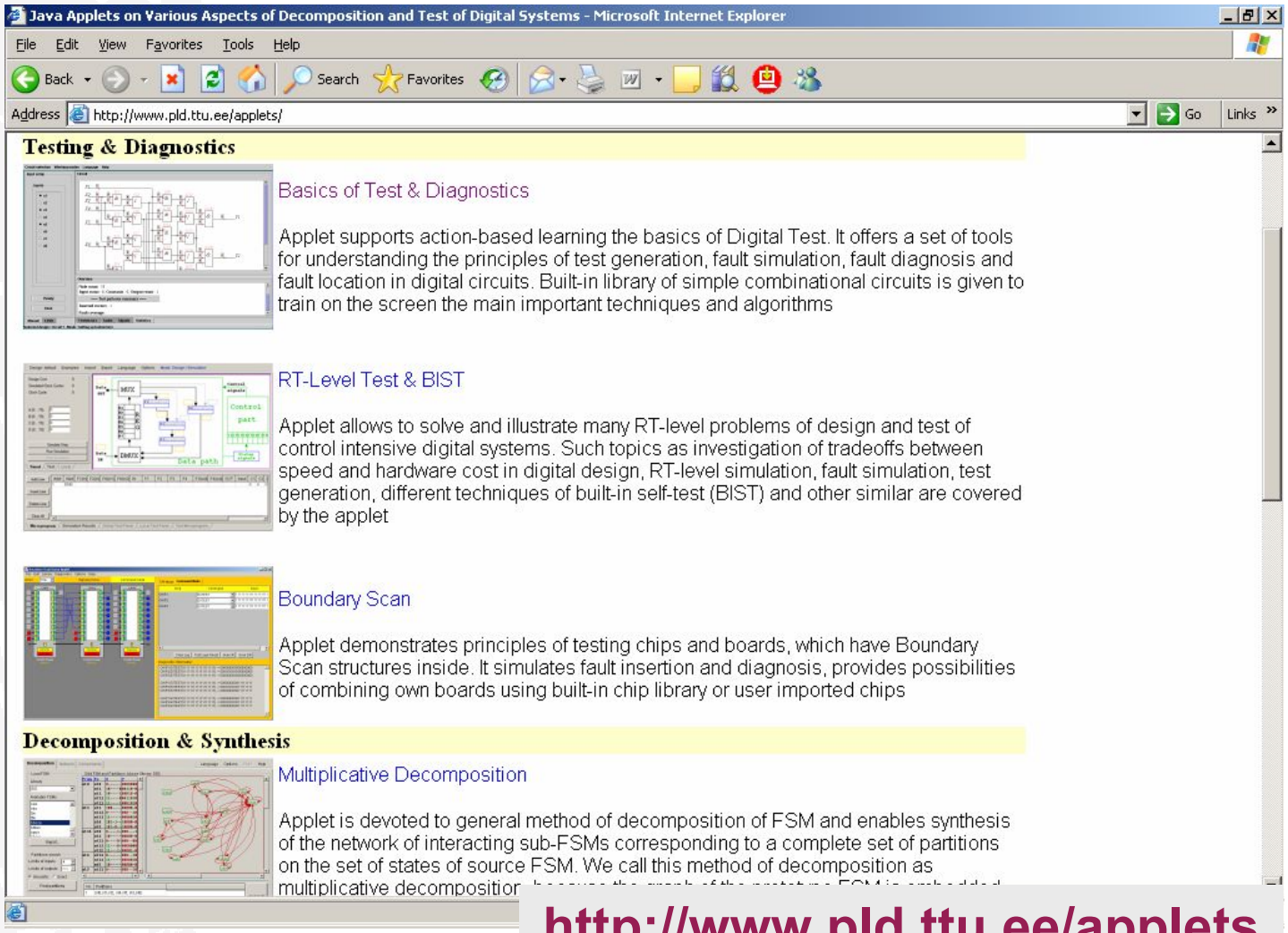




Hardware Tools

E-Learning software on DFT



http://www.pld.ttu.ee/applets

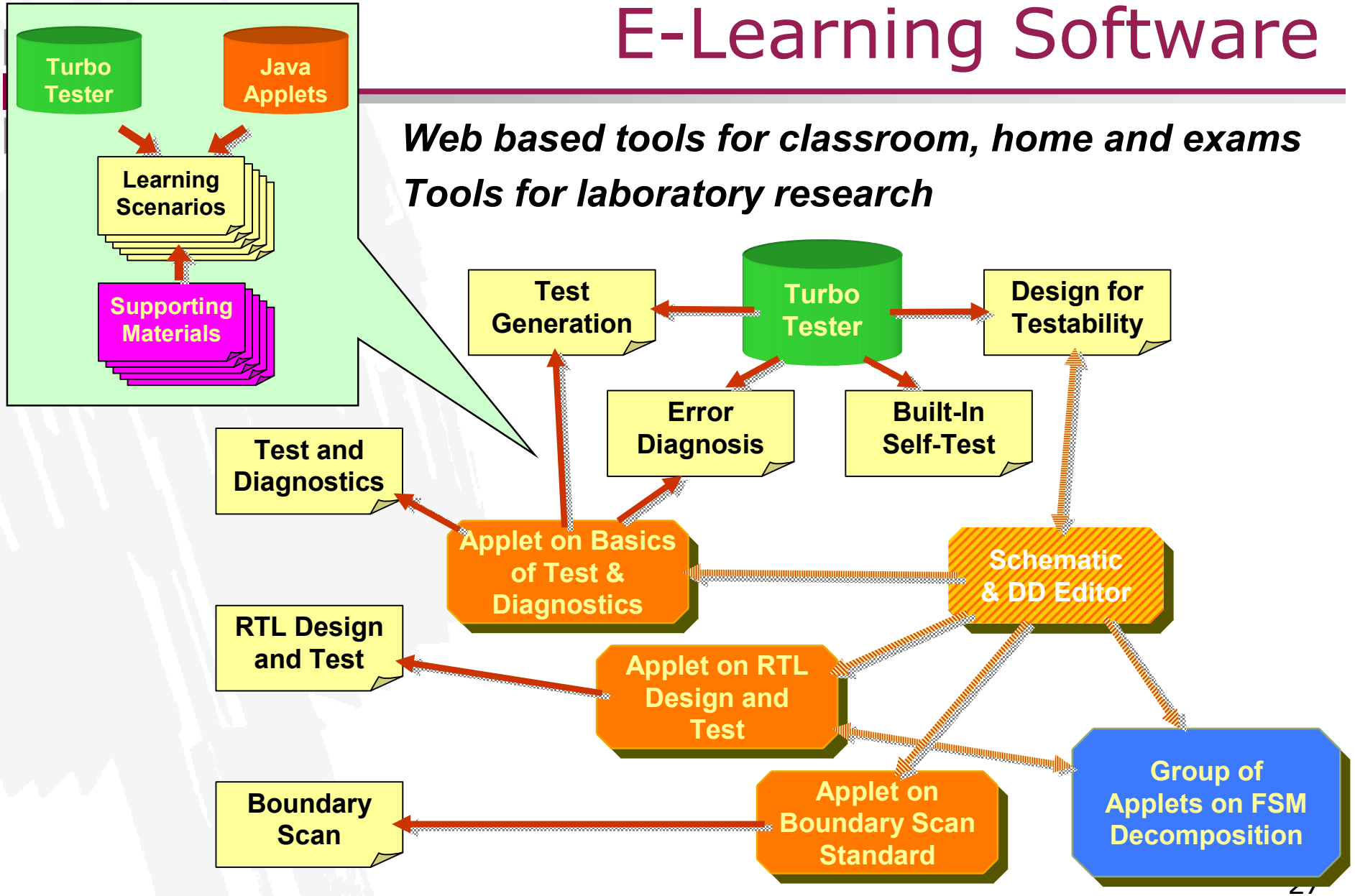
Benefits of e-learning software

- ✓ Essential supplement to the university lectures
- ✓ Accessibility over Internet
- ✓ Visual content
- ✓ Comprehensive examples
- ✓ Better organization of teaching materials
- ✓ Based on free educational software
- ✓ Distance learning & computer aided teaching
- ✓ Easy to implement in other universities
- ✓ Constantly updated

E-Learning Software

Web based tools for classroom, home and exams

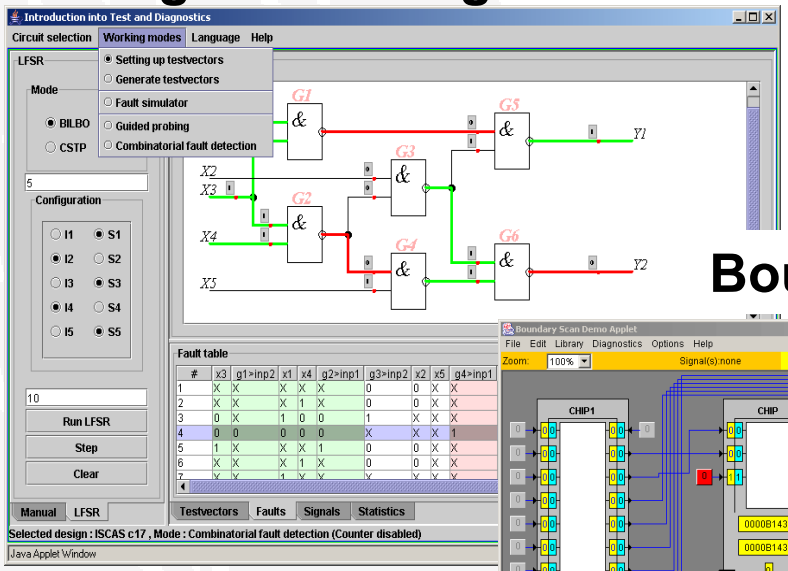
Tools for laboratory research



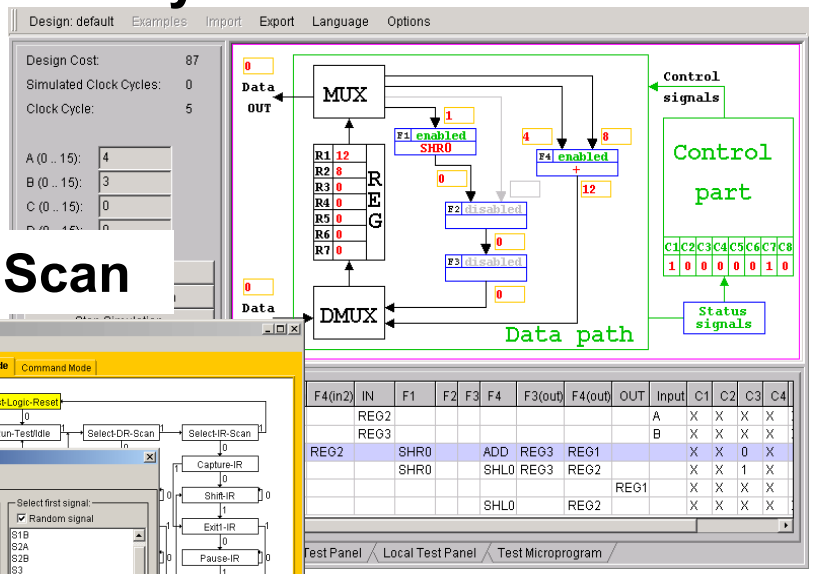
E-Learning Software

Software for classroom, home, labs and exams:

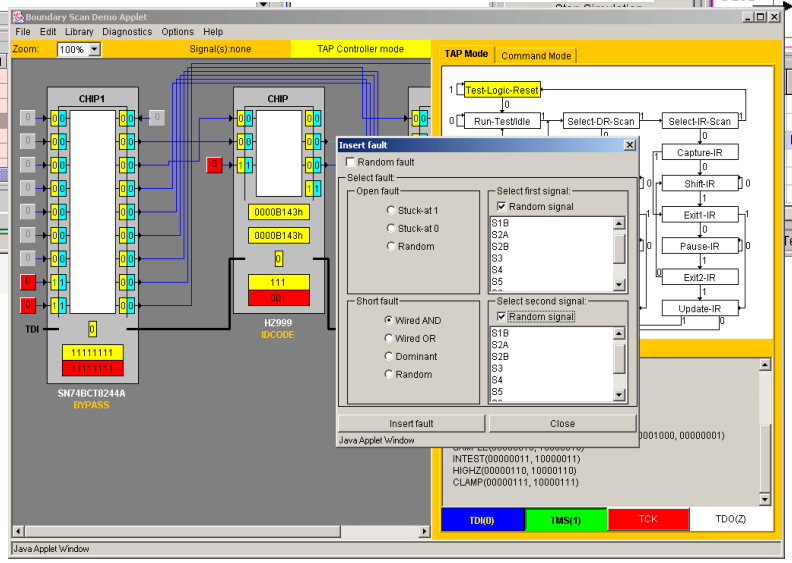
Logic level diagnostics



System level test & DfT



Boundary Scan



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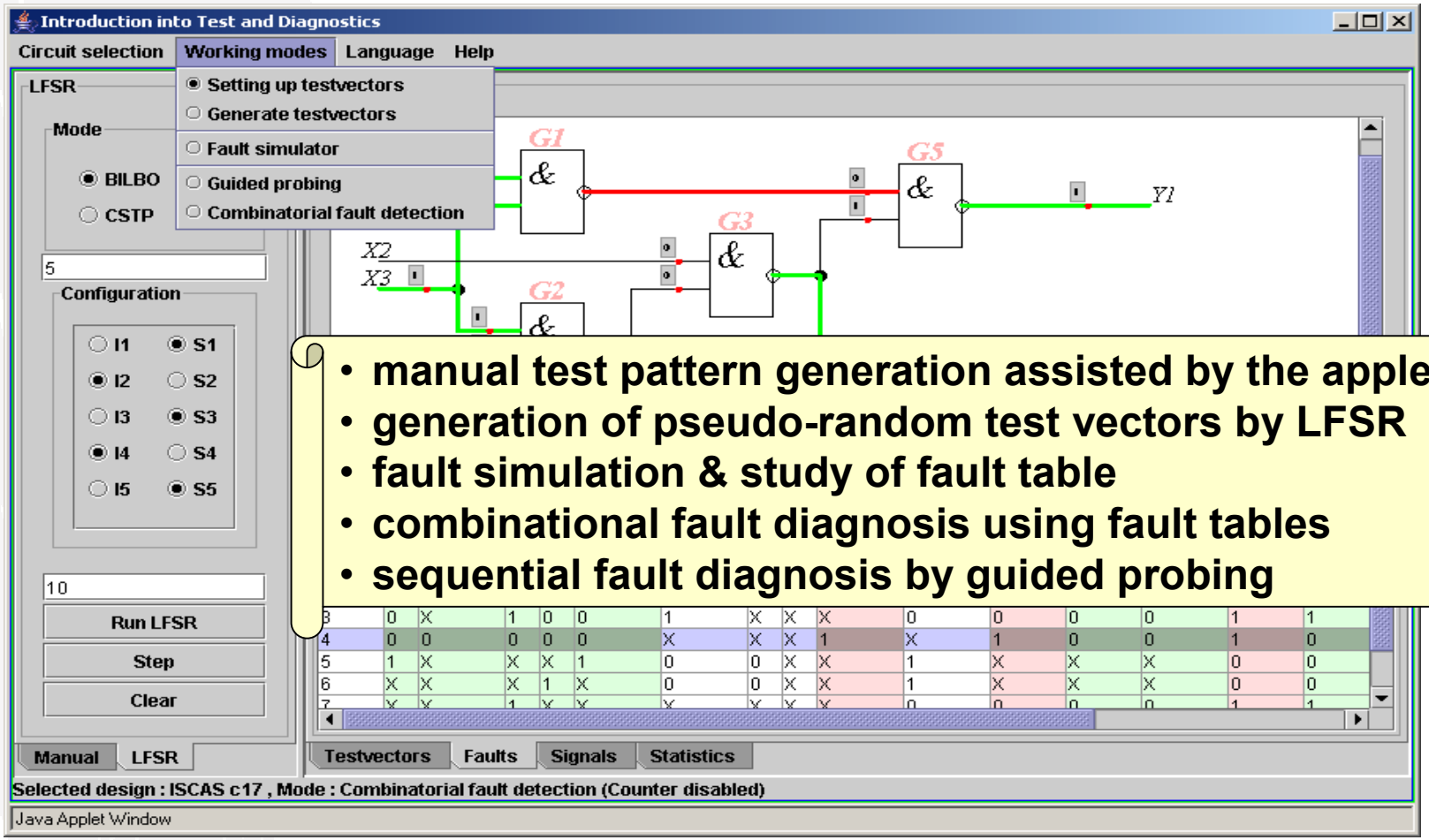
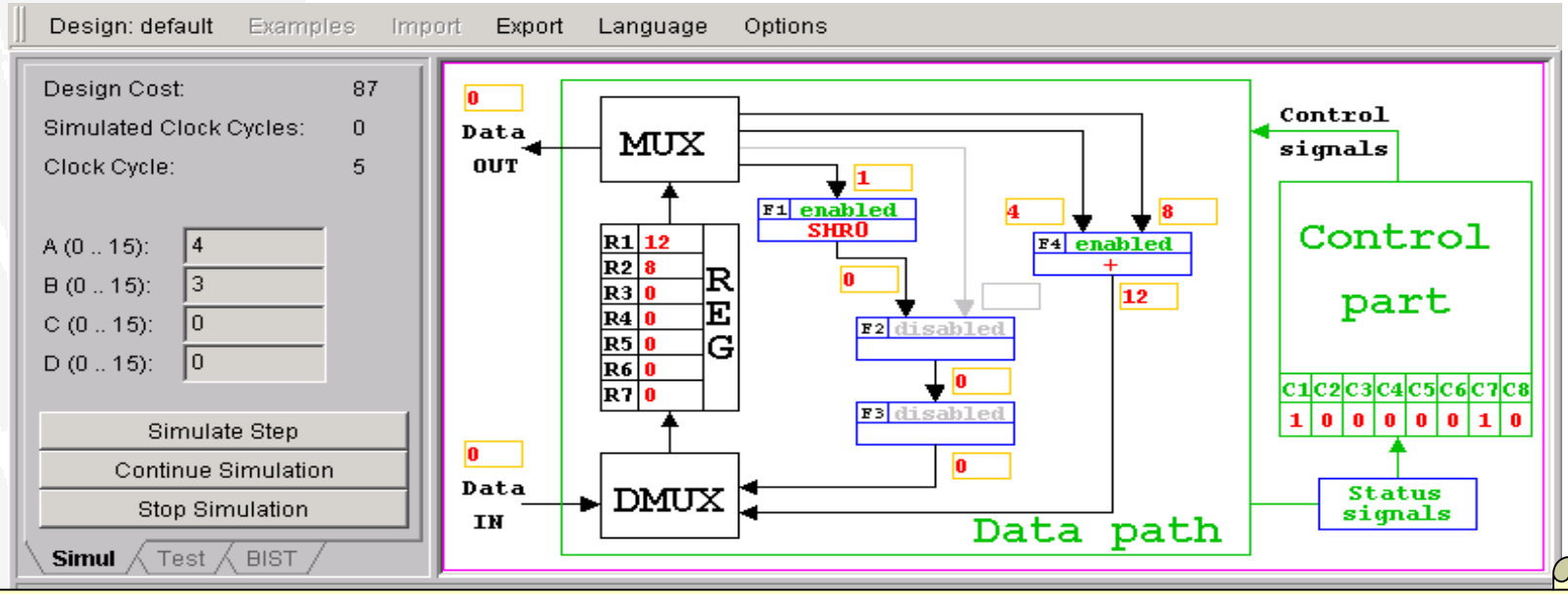
Applet on basics of test



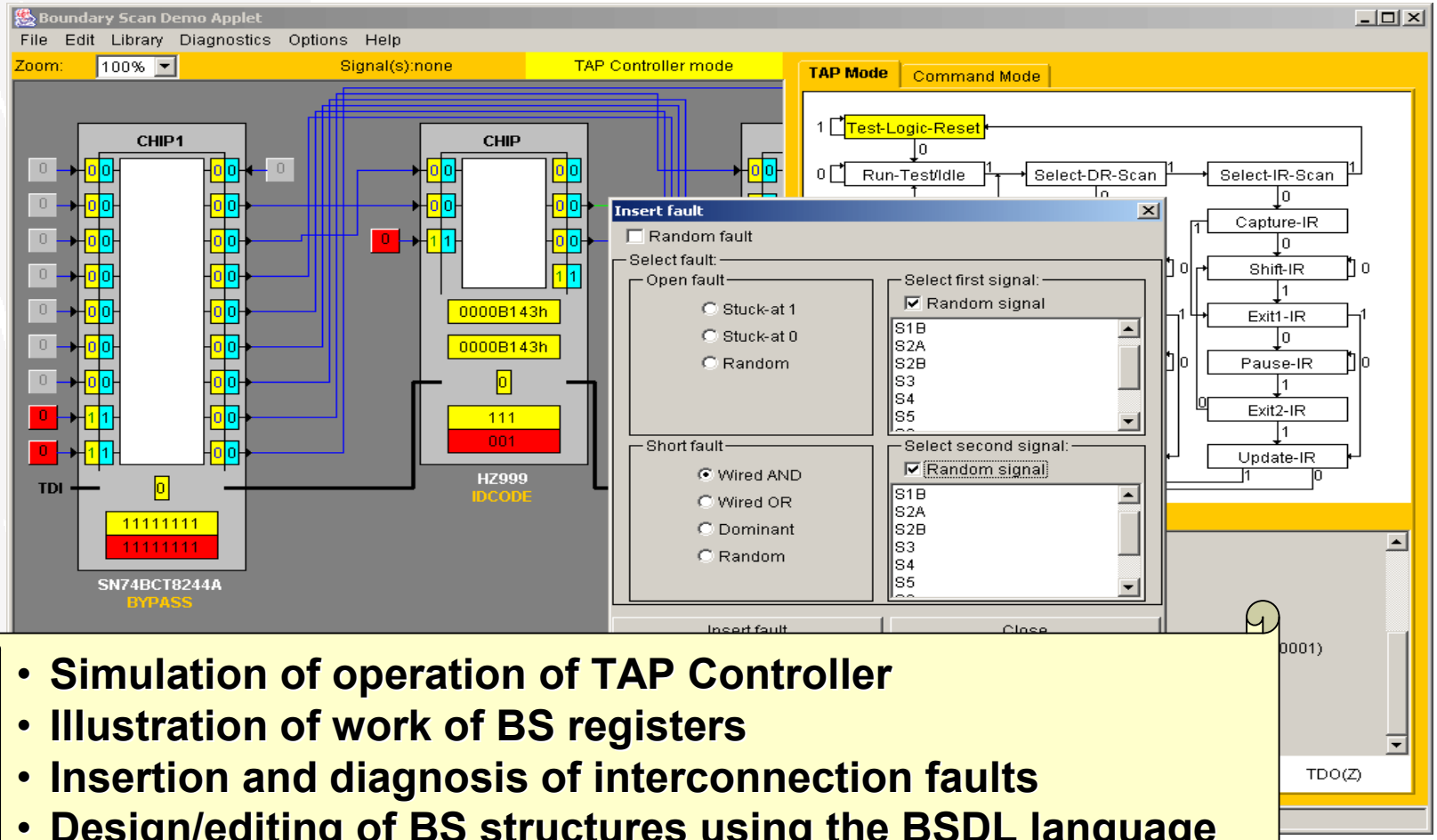
- manual test pattern generation assisted by the applet
- generation of pseudo-random test vectors by LFSR
- fault simulation & study of fault table
- combinational fault diagnosis using fault tables
- sequential fault diagnosis by guided probing

Applet on RT-level design and test



- design of a data path and control path (microprogram) on RT level
- investigation of tradeoffs between speed of the system & HW cost
- RT-level simulation and validation
- gate-level deterministic test generation and functional testing
- fault simulation
- logic and circular BIST, functional BIST, etc.
- design for testability

Applet on Boundary Scan



- **Simulation of operation of TAP Controller**
- **Illustration of work of BS registers**
- **Insertion and diagnosis of interconnection faults**
- **Design/editing of BS structures using the BSDL language**
- **Design/description of the target board using several chips**

Schematic and DD editor

Main functions of the applet are:
- **gate-level schematic editor**
- **SSBDD editor**
- **schematic ↔ SSBDD on-the-fly converter**
- **different format reader/converter**

Design for Testability

An applet targeted at binding all the applets and the Turbo Tester

AGM, GIF

Schematic & DD Editor

AGM, DWG

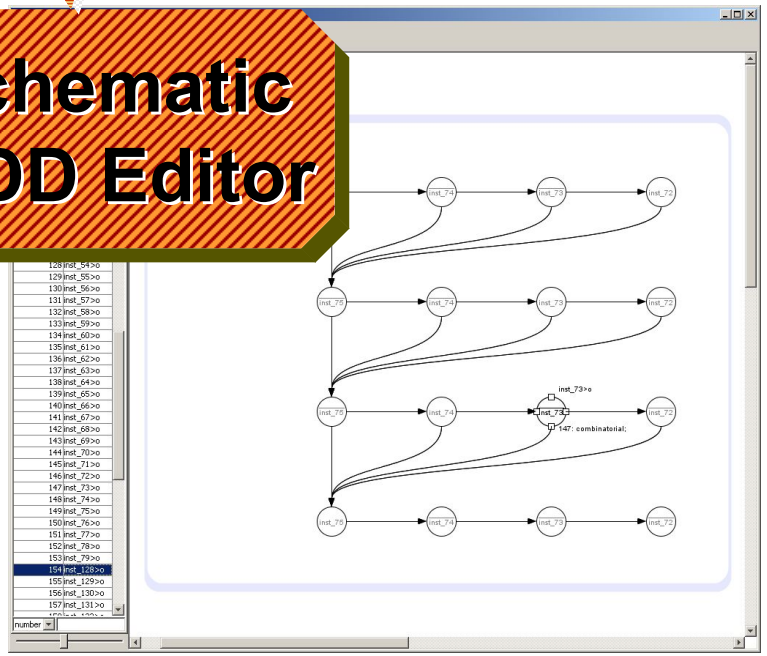
Applet on Basics of Test & Diagnostics

AGM, GIF

Applet on RTL Design and Test

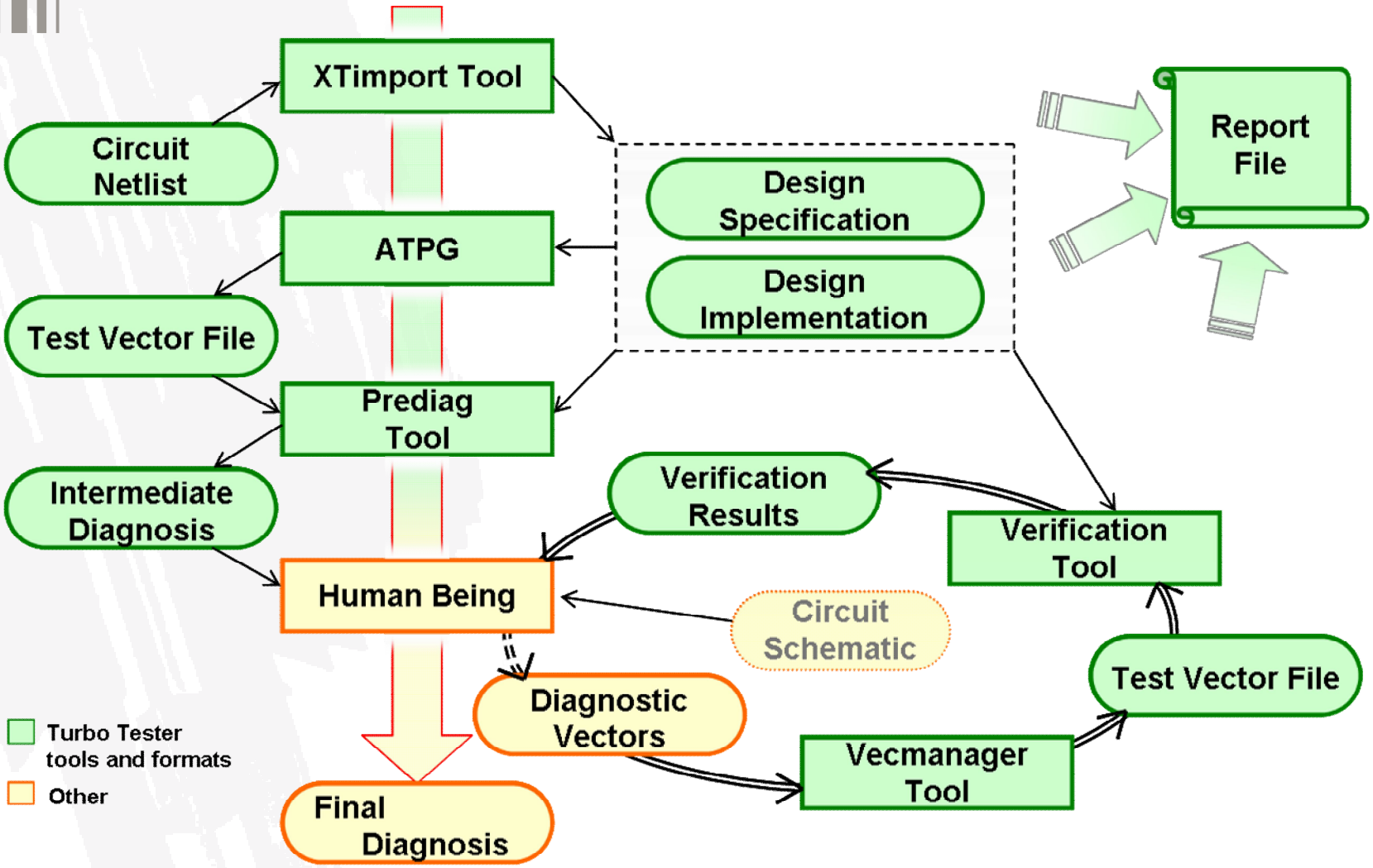
AGM

Applet on Boundary Scan Standard



It is still a work in progress!

Example of a lab work scenario



Conclusions & Discussion

The main features of the platform:

- Research engine + training software
- Layered structure
- HW and SW components
- Remote access
- Distance learning and e-learning
- Computer-aided teaching
- Freeware

Our Tools on the Web

The Turbo Tester home page

http://www.pld.ttu.ee/tt/

The Turbo Tester web-server page

http://www.pld.ttu.ee/webtt/

DefSim web-server page

http://www.defsim.com

Java applets home page

http://www.pld.ttu.ee/applets/