




A multi-layer research and training platform for system-on-chip testing: *Hardware, Software and Web Interface*

Artur Jutman

Dept. of Computer Engineering
Tallinn University of Technology
Estonia





Outline

- ✓ Introduction and motivation
- ✓ Different layers of the platform
- ✓ HW tools
- ✓ PC-based tools
- ✓ Web interface
- ✓ E-Learning tools
- ✓ Conclusions and discussion

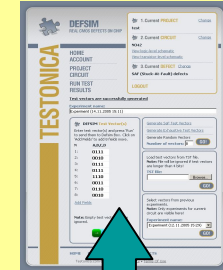
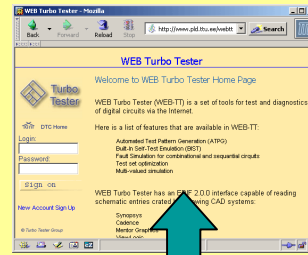
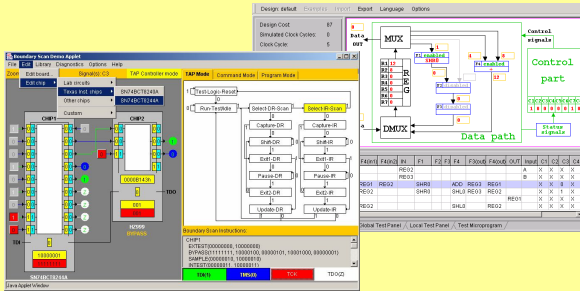


Motivation

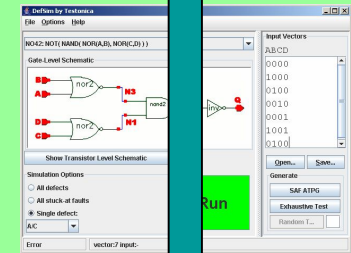
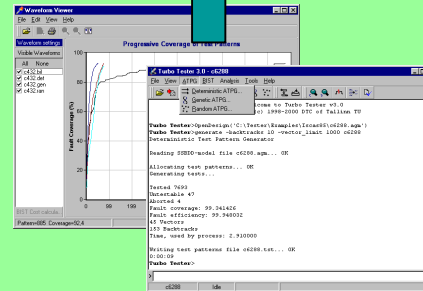
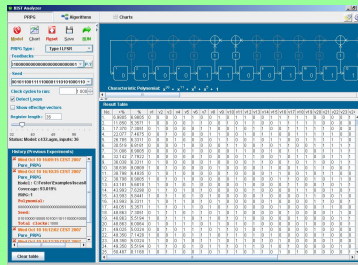
- ✓ **Cutting Edge Research**
 - Needs custom developed algorithms and/or tools
- ✓ **PhD Students**
 - Need to run their experiments
- ✓ **Undergraduate Students**
 - Need introduction to the topic
- ✓ **Department**
 - Needs training materials and research

Different layers of the platform

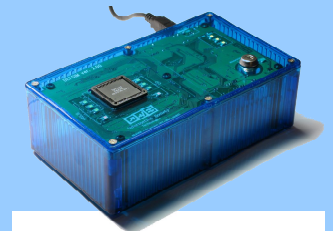
Web Tools



PC Tools

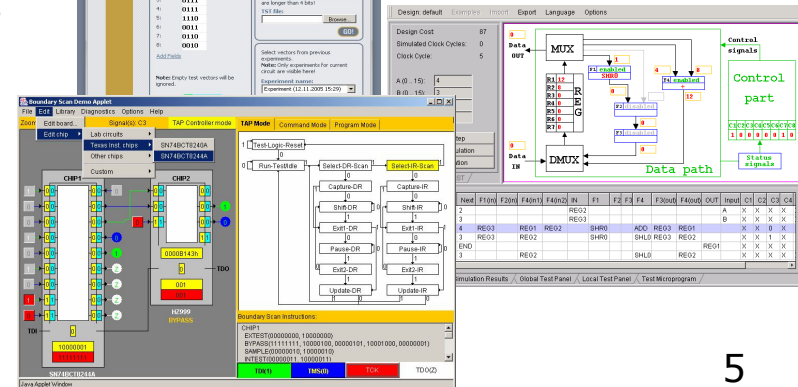
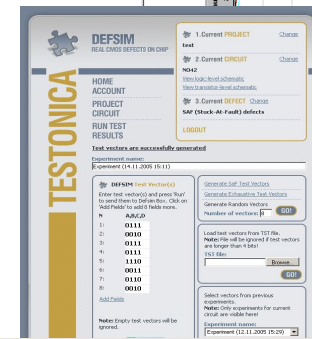
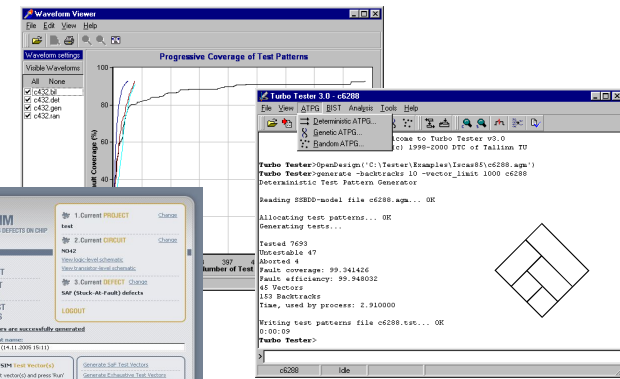
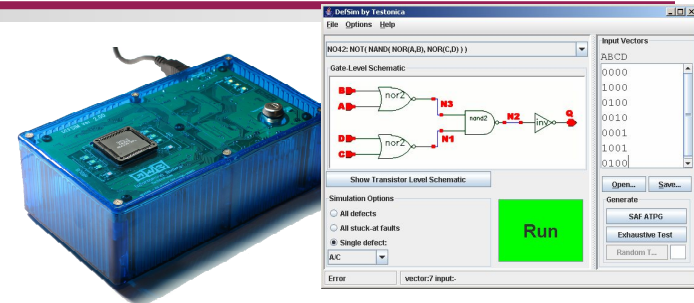


Hardware Tools



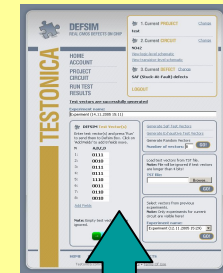
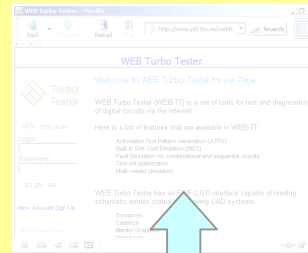
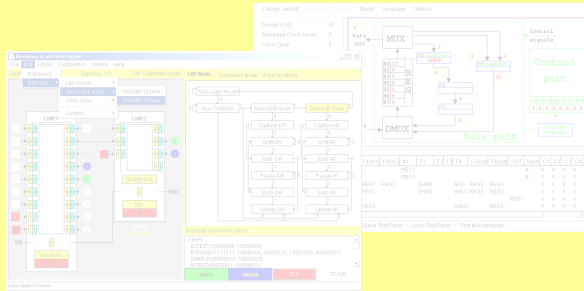
Main components of the platform

- ✓ **DefSim** - an integrated measurement environment for physical defect study in CMOS circuits.
- ✓ **TurboTester** – a research and training toolkit with extensive set of tools for digital test and design for testability
- ✓ **Web-based runtime interface** for remote access to our tools
- ✓ **Java applets** – illustrative e-learning software written specifically for the web
- ✓ **Other tools**

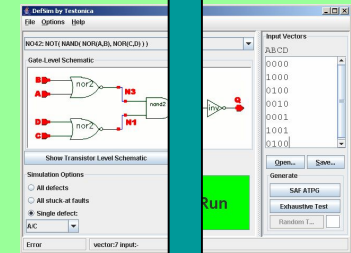
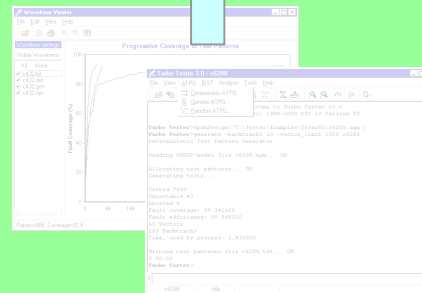
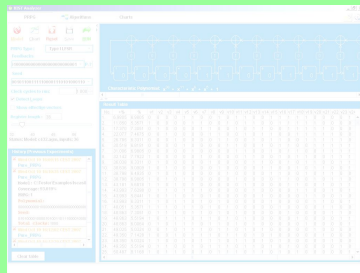


Different layers of the platform

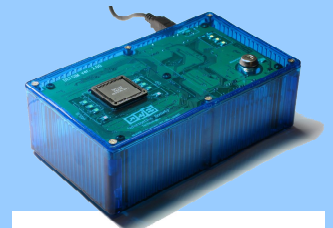
Web Tools



PC Tools



Hardware Tools



Defect Study using DefSim

- ✓ DefSim is an **integrated circuit** (ASIC) and a measurement equipment for experimental study of CMOS defects.
- ✓ The central element of the DefSim equipment is an educational IC with a **large variety of shorts and opens** physically inserted into a set of simple digital circuits.
- ✓ The IC is attached to a dedicated measurement box serving as an interface to the computer. The box supports two measurement modes - **voltage** and **I_{DDQ} testing**.

The image displays the DefSim software interface and its hardware components. The software window, titled "DefSim by Testonica", shows a "HOME ACCOUNT PROJECT CIRCUIT RUN TEST RESULTS" menu. The "PROJECT CIRCUIT" section displays "NO42" and "SAF (Stuck-At-Fault) defects". The "RUN TEST RESULTS" section shows "Test vectors are successfully generated" and "Experiment name: Experiment (14.11.2005 15:11)".

The hardware components include a black integrated circuit (IC) labeled "DefSim2 EDUCATIVE REASON-42" and a blue measurement box with a green PCB and a chip. The measurement box is connected to the IC.

The software interface also shows a "DEFSIM Test Vector(s)" section with a table of test vectors:

| N | A,B,C,D |
|----|---------|
| 1: | 0111 |
| 2: | 0010 |
| 3: | 0111 |
| 4: | 0111 |
| 5: | 1110 |
| 6: | 0011 |
| 7: | 0110 |
| 8: | 0010 |

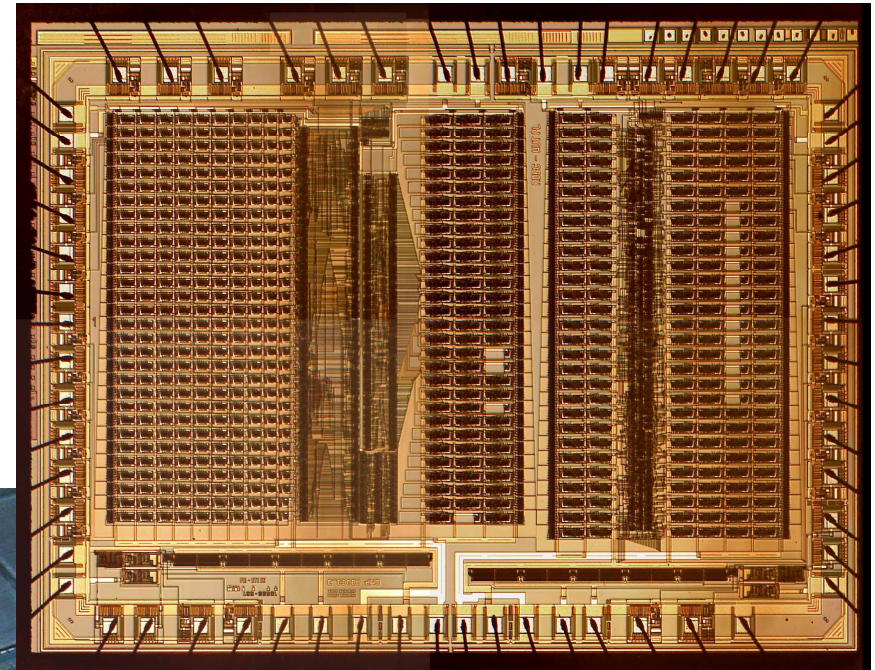
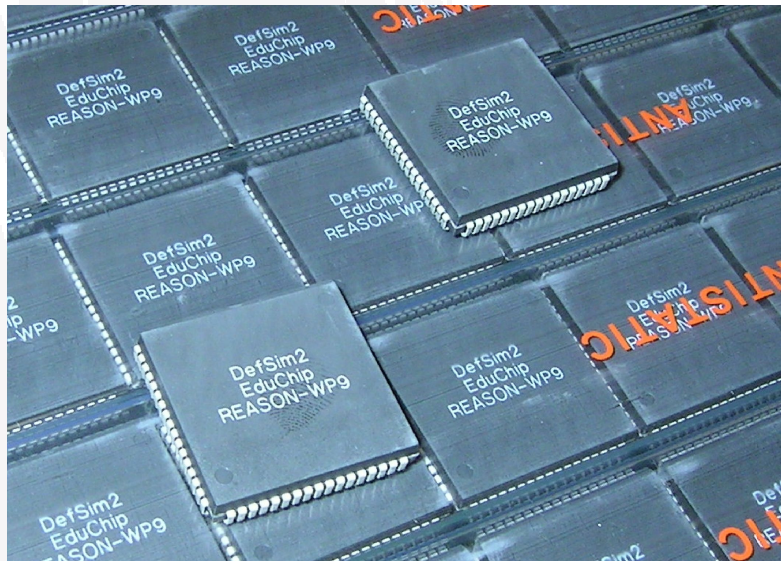
The "Gate-Level Schematic" section shows a circuit diagram with two NOR gates (nor2) and one NAND gate (nand2). The NOR gates have inputs B,D and A,D, and outputs N3 and N1. The NAND gate has inputs N3 and N1, and output N2. The output N2 is connected to an inverter (inv) with output Q. The circuit is labeled "NO42: NOT(NAND(NOR(A,B), NOR(C,D)))".

The "Simulation Options" section shows "All defects", "All stuck-at faults", and "Single defect:" (selected). The "A/C" dropdown is set to "A/C". The "Run" button is highlighted in green.

The "Generate" section shows "SAF ATPG", "Exhaustive Test", and "Random T..." buttons. The "Error" section shows "vector:7 input:-".

DefSim IC details

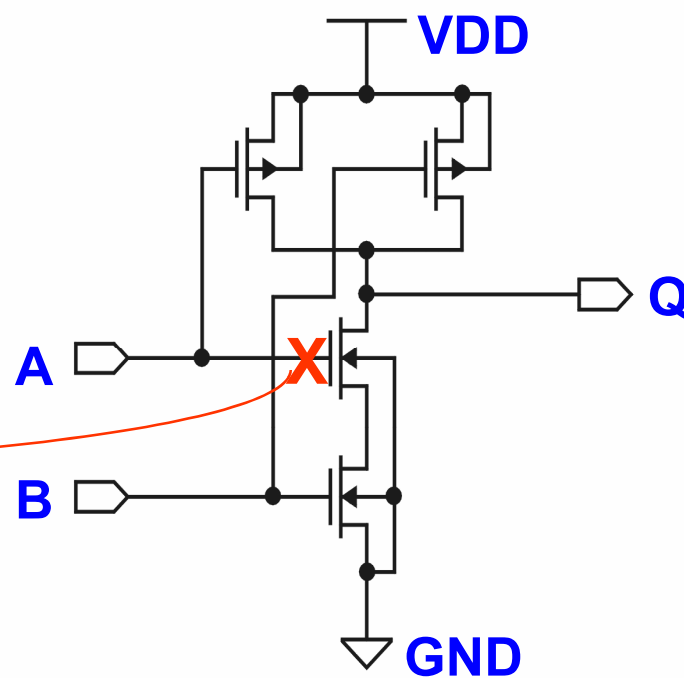
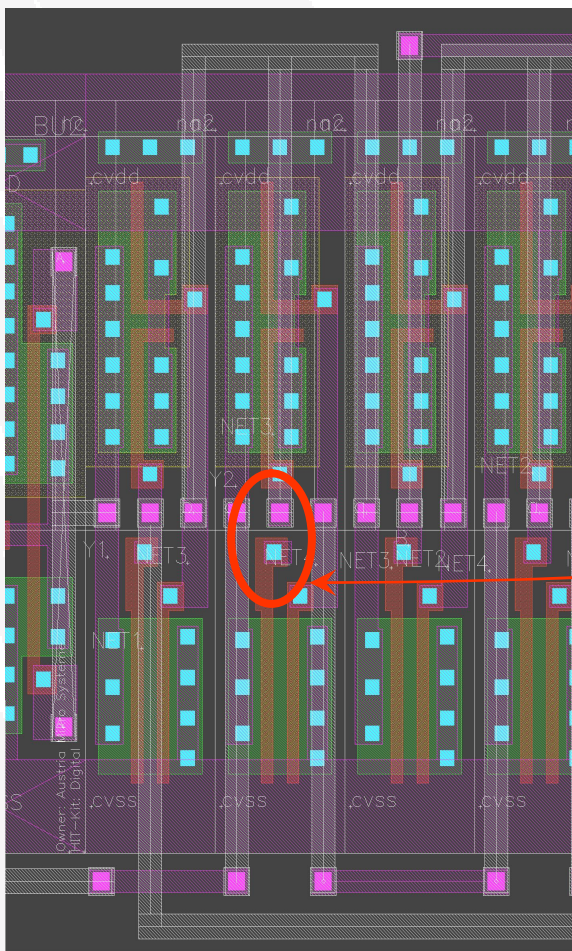
- Standard industrial CMOS technology
- Area 19.90 mm²
- Approx. 48000 transistors
- 62 pins
- JLCC68 package



A built-in current monitor for I_{DDQ} testing is implemented in each block.

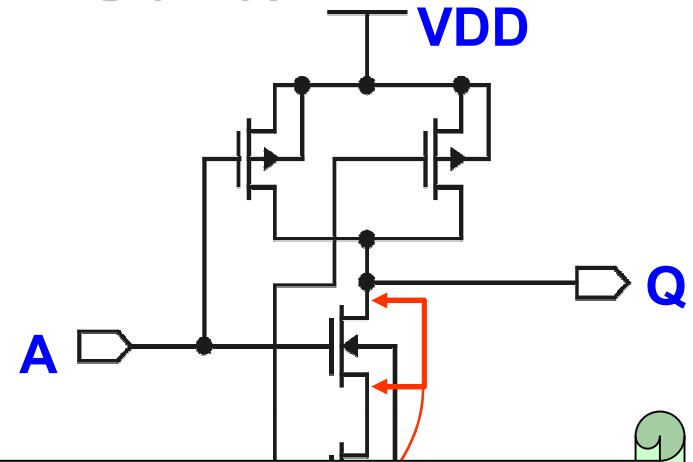
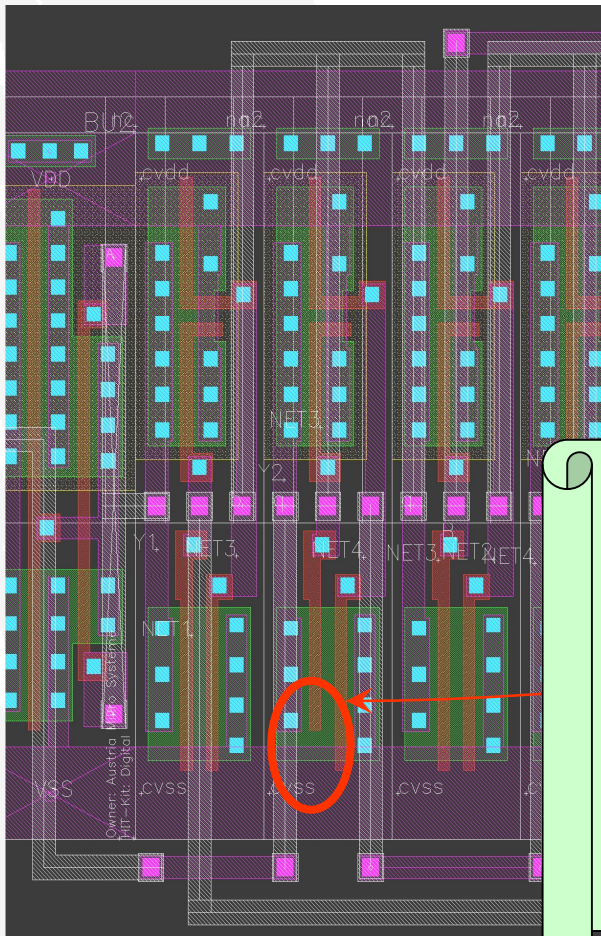
Implementation of defects

NAND2 cell with floating gate



Implementation of defects

NAND2 cell with D-S short (missing poly)



- Altogether there are over 500 different defects on the chip
- Implemented defects are shorts and opens in metal and poly layers
- To be close to the silicon reality each cell is loaded and driven by standard non-inverting buffers

DefSim in the classroom

- ✓ *With DefSim you can*
- ✓ Observe the truth table of correct circuit
- ✓ Observe the truth table of defective circuit
- ✓ Obtain defect/fault tables for all specific defects
- ✓ Define test patterns automatically or manually
- ✓ Activate IDDQ and voltage measurements
- ✓ Study behavior of bridging and open faults
- ✓ Study and compare different fault models

DefSim lab environment



“Plug and Play” – dedicated hardware and software

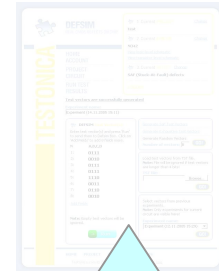
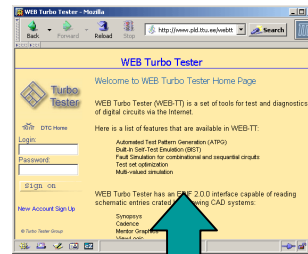
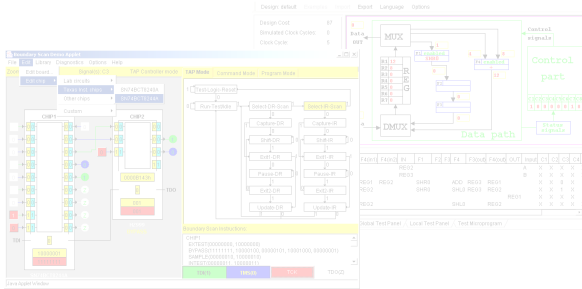
DefSim user interface

The image displays the DefSim user interface through several overlapping screenshots:

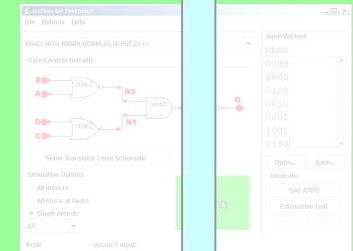
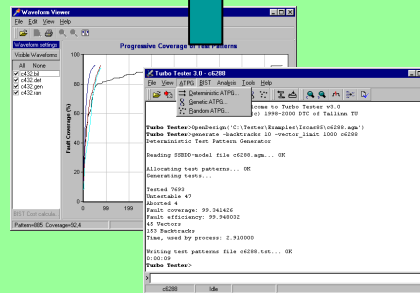
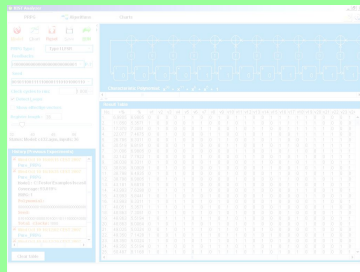
- Adobe Reader:** Shows a PDF document titled "Experiment results 20:49:38, page 1 [ON1, single defect: n1/Q, Iddq activated]". It contains a table of test results for various DCBA inputs and Q outputs.
- DefSim (Main Window):** Shows a logic schematic for the function $ON1 = NAND(OR(A,B), OR(C,D))$. It includes a "Fault table" with columns for defects (A/B, A/C, A/gnd, A/Q, A/vdd, B/C, B/gnd, B/Q, B/vdd, C/gnd, C/Q, C/vdd, Q/gnd, Q/vdd, Q) and rows for input vectors (0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111). A "Run" button is prominently displayed in green.
- DefSim Test Vector(s) Window:** Shows a list of test vectors (N, D,C,B,A) and their corresponding values (e.g., 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111).
- DefSim Web Interface:** Shows a web-based control panel with sections for "HOME ACCOUNT PROJECT", "RUN TEST RESULTS", and "DEFMIM Test Vector(s)". It includes options to generate test vectors, load test files, and execute tests.

Different layers of the platform

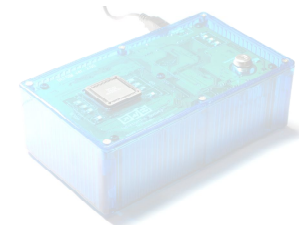
Web Tools



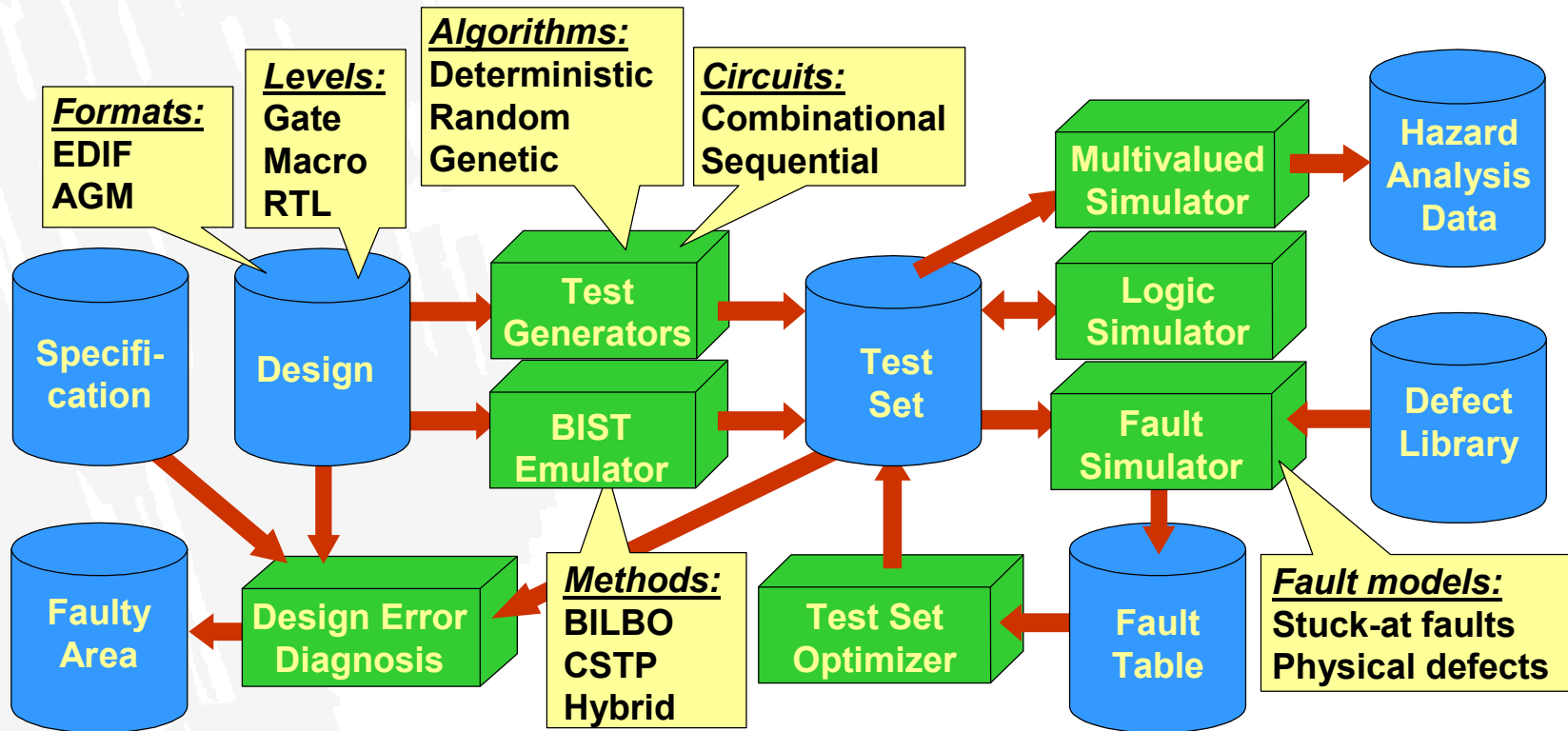
PC Tools



Hardware Tools



PC-Based Toolkit – Turbo Tester



Turbo Tester's user interface

```

Turbo Tester 3.0 - c6288
File View ATPG BIST Analysis Tools Help
Welcome to Turbo Tester v3.0
(c) 1998-2000 DTC of Tallinn TU

Turbo Tester>OpenDesign('C:\Tester\Examples\Iscas85\c6288.agm')
Turbo Tester>generate -backtracks 10 -vector_limit 1000 c6288
Deterministic Test Pattern Generator

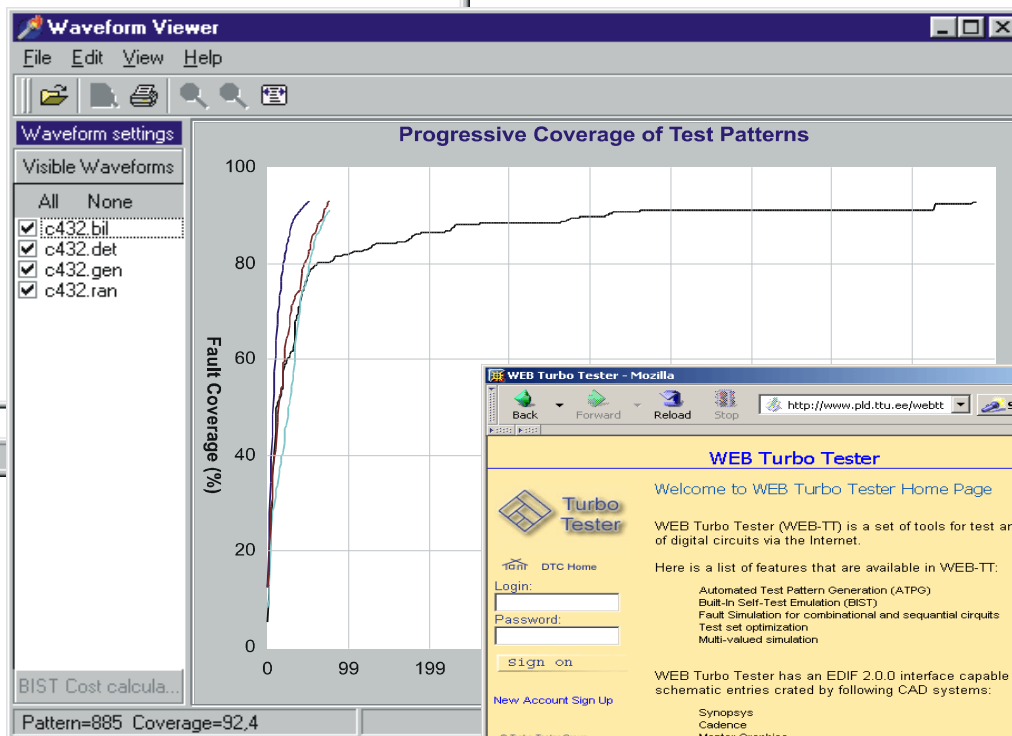
Reading SSBDD-model file c6288.agm... OK

Allocating test patterns... OK
Generating tests...

Tested 7693
Untestable 47
Aborted 4
Fault coverage: 99.341426
Fault efficiency: 99.948032
45 Vectors
153 Backtracks
Time, used by process: 2.910000

Writing test patterns file c6288.tst... OK
0:00:09
Turbo Tester>

```



WEB Turbo Tester - Mozilla

Back Forward Reload Stop http://www.pld.ttu.ee/webtt Search

WEB Turbo Tester

Welcome to WEB Turbo Tester Home Page

WEB Turbo Tester (WEB-TT) is a set of tools for test and diagnostics of digital circuits via the Internet.

Here is a list of features that are available in WEB-TT:

- Automated Test Pattern Generation (ATPG)
- Built-In Self-Test Emulation (BIST)
- Fault Simulation for combinational and sequential circuits
- Test set optimization
- Multi-valued simulation

WEB Turbo Tester has an EDIF 2.0.0 interface capable of reading schematic entries created by following CAD systems:

Synopsys
Cadence
Mentor Graphics

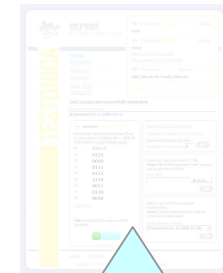
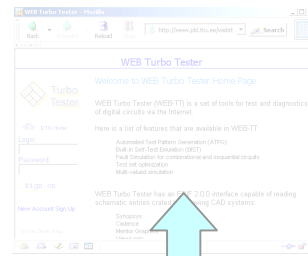
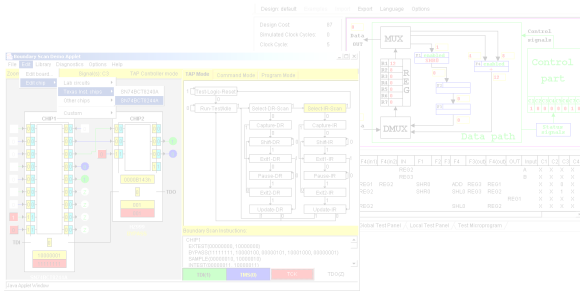
© Turbo Tester Group

Turbo Tester: Basic Facts

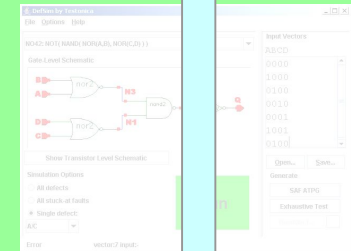
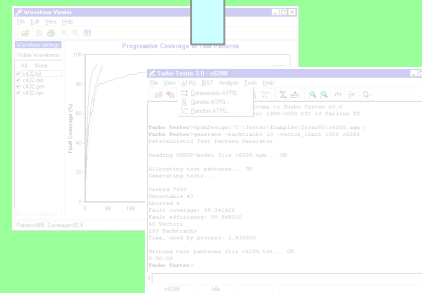
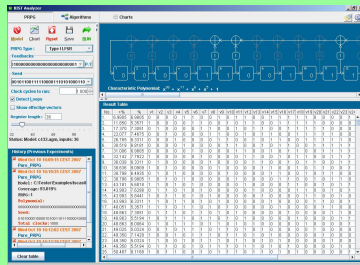
- ✓ Freeware
- ✓ Downloadable via the Web
- ✓ Windows, Linux, UNIX/Solaris
- ✓ EDIF design interface
- ✓ ATPGs, BIST, simulators, test compaction
- ✓ Provides homogeneous environment for research and training

Different layers of the platform

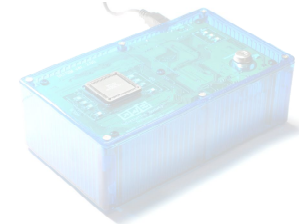
Web Tools



PC Tools



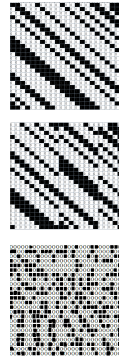
Hardware Tools



BIST Analyzer: covered topics

✓ Test Pattern Generators (PRPG):

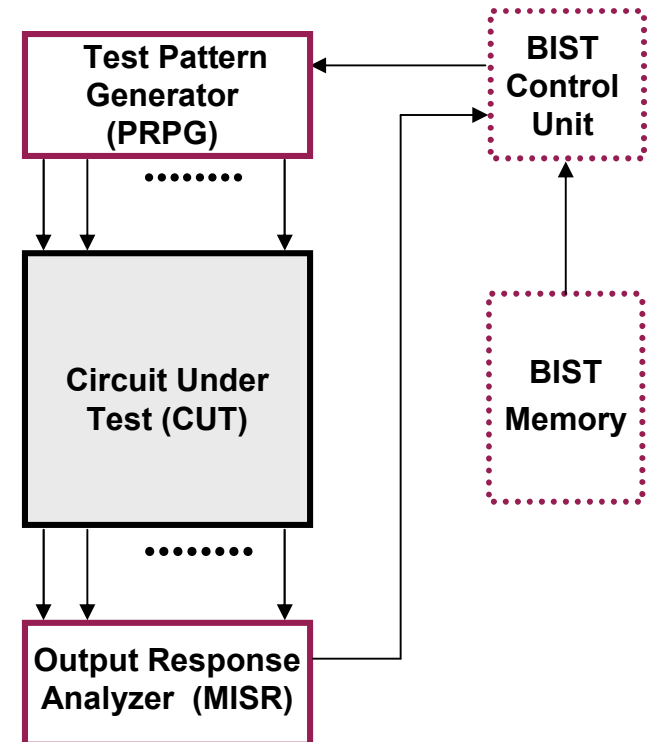
- LFSR
- Modular LFSR
- Cellular Automata
- *GLFSR*
- *Weighted TPG*
- *etc.*



✓ Combined Techniques (PRPG + Memory):

- Reseeding
- Multiple polynomial BIST
- Hybrid BIST
- *Bit-Flipping BIST*
- *Column matching BIST*
- *etc.*

Typical BIST Architecture





BIST Analyzer: covered topics

- Different embedded generators (PRPG) and their properties
- PRPG optimization methodologies and algorithms
- Mixed-mode BIST solutions (PRPG+memory)
- Fault detection and diagnosis in BIST

BIST Analyzer

BIST Analyzer

PRPG Algorithms Charts

Model Chart Reset Save RUN

PRPG Type: Type I LFSR

Feedbacks: 11000000000000000000000000000000000000000001 P-?

Seed: 001011001111100001110101000110

Clock cycles to run: 1,000

Detect Loops

Show effective vectors

Register length: 36

Status: Model: c432.agm, inputs: 36

Characteristic Polynomial: $x^{36} + x^{11} + x^6 + x^5 + 1$

Result Table

| No. | +% | % | v1 | v2 | v3 | v4 | v5 | v6 | v7 | v8 | v9 | v10 | v11 | v12 | v13 | v14 | v15 | v16 | v17 | v18 | v19 | v20 | v21 | v22 | v23 | v24 |
|-----|--------|--------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1. | 6.9805 | 6.9805 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 2. | 11.850 | 5.3571 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 3. | 17.370 | 7.3051 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 4. | 22.077 | 7.4675 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 5. | 26.785 | 6.3311 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 6. | 30.519 | 6.8181 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 7. | 31.006 | 6.9805 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 8. | 32.142 | 7.7922 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 9. | 36.038 | 6.3311 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 10. | 38.636 | 9.0909 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11. | 38.798 | 6.4935 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12. | 38.798 | 6.9805 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13. | 43.181 | 5.6818 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14. | 43.993 | 7.6298 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15. | 43.993 | 5.8441 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16. | 43.993 | 6.3311 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17. | 48.051 | 5.3571 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 18. | 48.863 | 7.3051 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 19. | 48.863 | 5.5194 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20. | 48.863 | 6.0064 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 21. | 49.025 | 5.0324 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 22. | 49.350 | 7.1428 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 23. | 49.350 | 5.0324 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 24. | 49.350 | 5.5194 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 25. | 50.487 | 8.1168 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Fault Coverage

Load TST Remove ALL Remove UNCHECKED

Waveforms

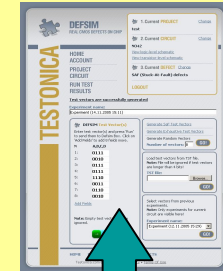
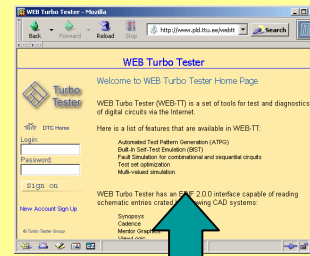
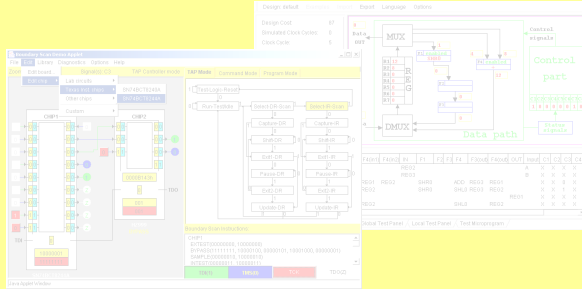
- M_PR (281)
- M_PR (281)
- M_PR (999)
- c432_ATPG
- M_PR (999)
- M_PR (999)

Fault Coverage (%) vs Time

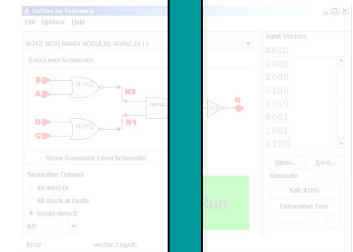
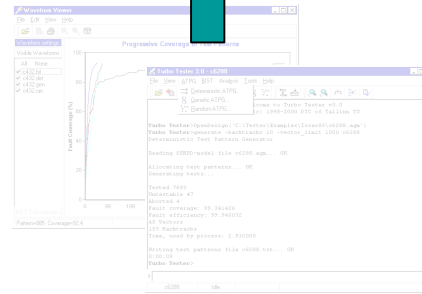
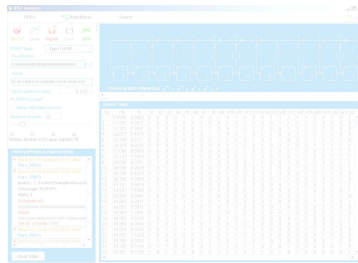
Legend: —M_PR (281) —M_PR (999) —c432_ATPG —M_PR (999) —M_PR (999)

Different layers of the platform

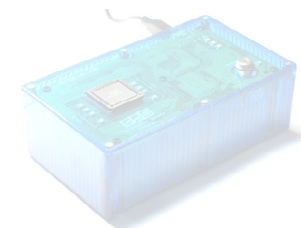
Web Tools



PC Tools



Hardware Tools



Web Interface

WEB Turbo Tester - Mozilla
 http://www.pld.ttu.ee/webtt

WEB Turbo Tester

Welcome to WEB Turbo Tester Home Page

Turbo Tester

WEB Turbo Tester (WEB-TT) is a set of tools for test of digital circuits via the Internet.

Here is a list of features that are available in WEB-TT:

- Automated Test Pattern Generation (ATPG)
- Built-In Self-Test Emulation (BIST)
- Fault Simulation for combinational and sequential circuits
- Test set optimization
- Multi-valued simulation

WEB Turbo Tester has an EDIF 2.0.0 interface capable of schematic entries created by following CAD systems:

- Synopsys
- Cadence
- Mentor Graphics
- View more...

© Turbo Tester Group

Navigation: Back, Forward, Reload, Stop

TESTONICA

DEFSIM
REAL CMOS DEFECTS ON CHIP

1. Current **PROJECT** [Change](#)
test

2. Current **CIRCUIT** [Change](#)
NO42
[View logic-level schematic](#)
[View transistor-level schematic](#)

3. Current **DEFECT** [Change](#)
SAF (Stuck-At-Fault) defects

[LOGOUT](#)

HOME ACCOUNT PROJECT CIRCUIT RUN TEST RESULTS

Test vectors are successfully generated

Experiment name:
Experiment (14.11.2005 15:11)

DEFSIM Test Vector(s)

Enter test vector(s) and press 'Run' to send them to Defsim Box. Click on 'Add Fields' to add 8 fields more.

| N | A,B,C,D |
|----|---------|
| 1: | 0111 |
| 2: | 0010 |
| 3: | 0111 |
| 4: | 0111 |
| 5: | 1110 |
| 6: | 0011 |
| 7: | 0110 |
| 8: | 0010 |

[Add Fields](#)

Note: Empty test vectors will be ignored.

[Run](#)

[Generate SaF Test Vectors](#)

[Generate Exhaustive Test Vectors](#)

Generate Random Vectors
Number of vectors: [GO!](#)

Load test vectors from TST file.
Note: File will be ignored if test vectors are longer than 4 bits!
TST file: [Browse...](#) [GO!](#)

Select vectors from previous experiments.
Note: Only experiments for current circuit are visible here!

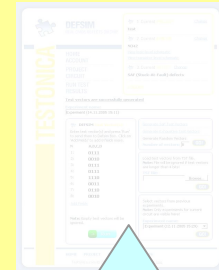
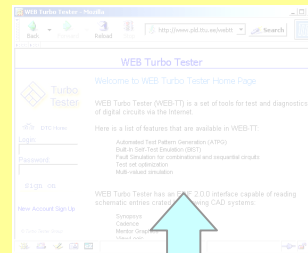
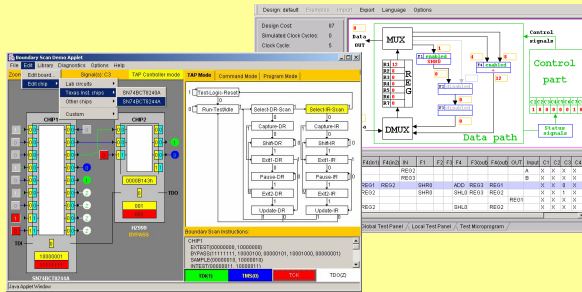
Experiment name:
Experiment (12.11.2005 15:29) [GO!](#)

HOME PROJECT ACCOUNT CONTACTS

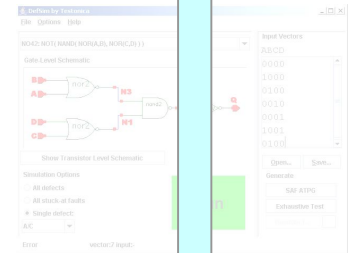
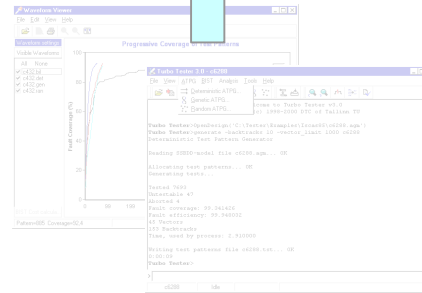
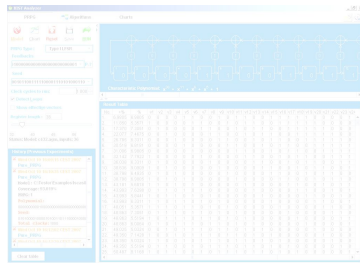
Testonica.com © 2005 • [Privacy Policy](#) • [Terms Of Use](#)

Different layers of the platform

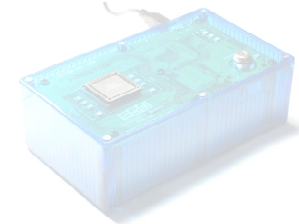
Web Tools



PC Tools



Hardware Tools



E-Learning software on DFT

Java Applets on Various Aspects of Decomposition and Test of Digital Systems - Microsoft Internet Explorer

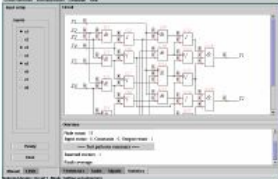
File Edit View Favorites Tools Help

Back Forward Stop Refresh Home Search Favorites

Address <http://www.pld.ttu.ee/applets/> Go Links

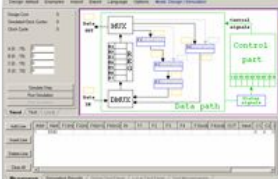
Testing & Diagnostics

Basics of Test & Diagnostics




Applet supports action-based learning the basics of Digital Test. It offers a set of tools for understanding the principles of test generation, fault simulation, fault diagnosis and fault location in digital circuits. Built-in library of simple combinational circuits is given to train on the screen the main important techniques and algorithms

RT-Level Test & BIST



Applet allows to solve and illustrate many RT-level problems of design and test of control intensive digital systems. Such topics as investigation of tradeoffs between speed and hardware cost in digital design, RT-level simulation, fault simulation, test generation, different techniques of built-in self-test (BIST) and other similar are covered by the applet


Boundary Scan



Applet demonstrates principles of testing chips and boards, which have Boundary Scan structures inside. It simulates fault insertion and diagnosis, provides possibilities of combining own boards using built-in chip library or user imported chips

Decomposition & Synthesis

Multiplicative Decomposition



Applet is devoted to general method of decomposition of FSM and enables synthesis of the network of interacting sub-FSMs corresponding to a complete set of partitions on the set of states of source FSM. We call this method of decomposition as multiplicative decomposition because the graph of the constructed FSM is constructed

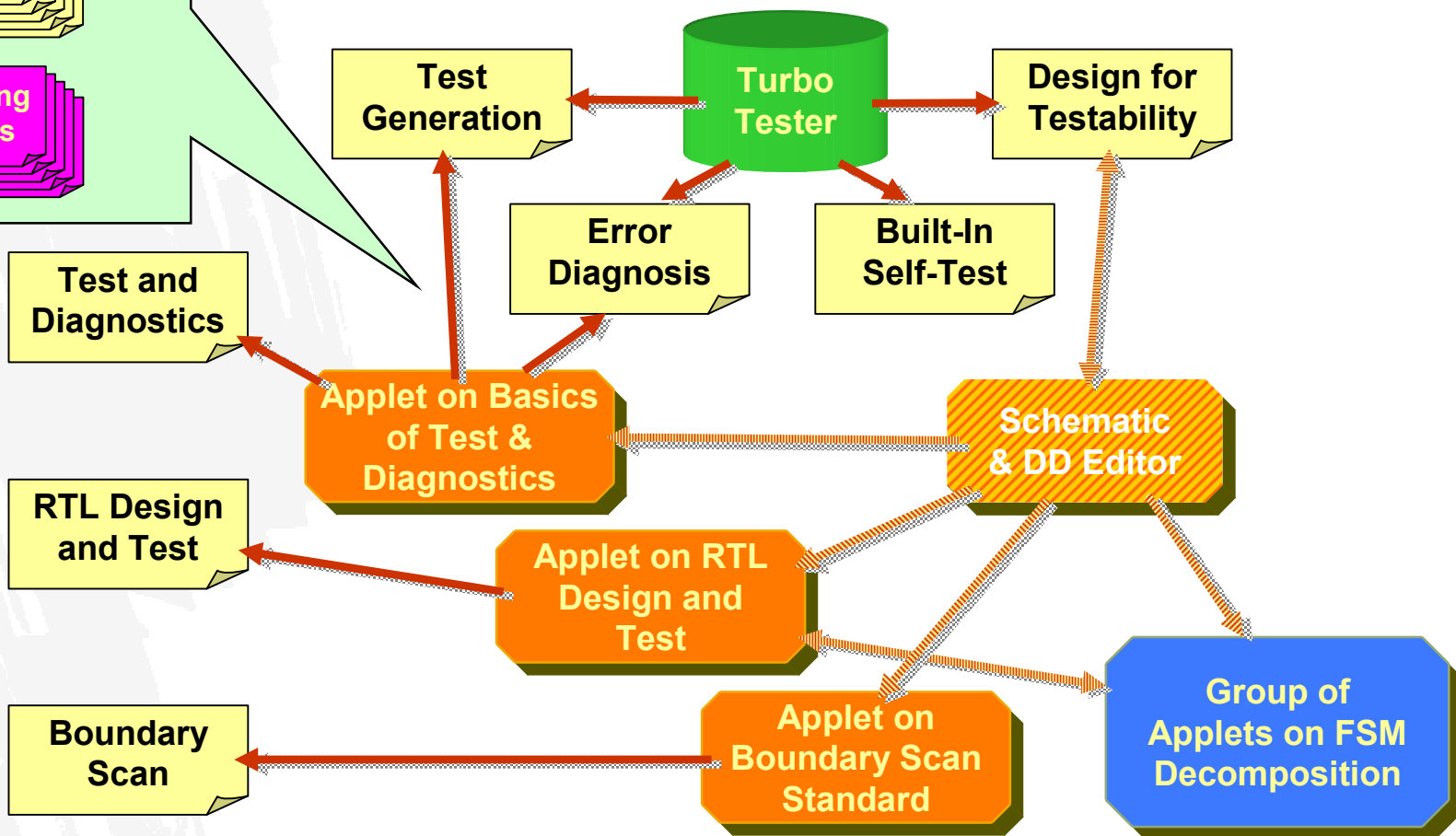
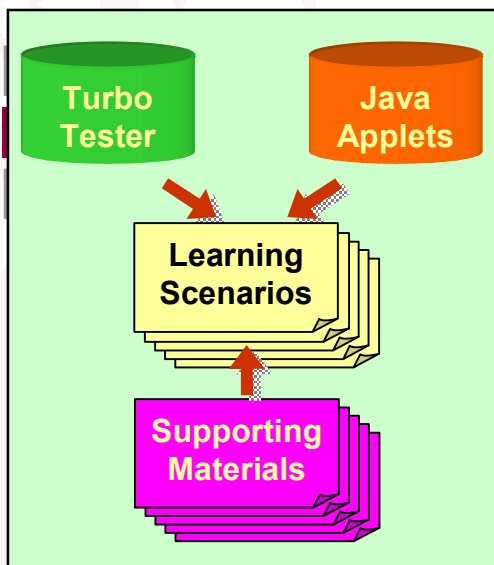
<http://www.pld.ttu.ee/applets>

Benefits of e-learning software

- ✓ Essential supplement to the university lectures
- ✓ Accessibility over Internet
- ✓ Visual content
- ✓ Comprehensive examples
- ✓ Better organization of teaching materials
- ✓ Based on free educational software
- ✓ Distance learning & computer aided teaching
- ✓ Easy to implement in other universities
- ✓ Constantly updated

E-Learning Software

Web based tools for classroom, home and exams
Tools for laboratory research



E-Learning Software

Software for classroom, home, labs and exams:

Logic level diagnostics

The screenshot shows a logic circuit with gates G1 through G6 and inputs X1 through X5. A fault table is displayed below the circuit.

| # | x3 | g1>inp2 | x1 | x4 | g2>inp1 | g3>inp2 | x2 | x5 | g4>inp1 |
|---|----|---------|----|----|---------|---------|----|----|---------|
| 1 | X | X | X | X | 0 | 0 | X | X | |
| 2 | X | X | X | 1 | X | 0 | X | X | |
| 3 | 0 | X | 1 | 0 | 0 | 1 | X | X | X |
| 4 | 0 | 0 | 0 | 0 | X | X | X | 1 | |
| 5 | 1 | X | X | X | 1 | 0 | 0 | X | X |
| 6 | X | X | X | 1 | X | 0 | 0 | X | X |
| 7 | X | X | 1 | X | X | X | X | X | X |

Selected design: ISCAS c17, Mode: Combinatorial fault detection (Counter disabled)

System level test & DfT

The screenshot shows a system-level circuit diagram with registers (R1-R7), a MUX, and a DMUX. Control signals (F1-F4) and status signals (C1-C8) are shown. A table below the diagram shows the status of various signals.

| F4(in2) | IN | F1 | F2 | F3 | F4 | F3(out) | F4(out) | OUT | Input | C1 | C2 | C3 | C4 |
|---------|------|----|------|------|------|---------|---------|-----|-------|----|----|----|----|
| REG2 | | | | | | | | | A | X | X | X | X |
| REG3 | | | | | | | | | B | X | X | X | X |
| REG2 | SHR0 | | ADD | REG3 | REG1 | | | | X | X | 0 | X | |
| | SHR0 | | SHL0 | REG3 | REG2 | | | | X | X | 1 | X | |
| | | | SHL0 | REG2 | REG1 | | | | X | X | X | X | |

Boundary Scan

The screenshot shows a Boundary Scan Demo Applet with a chip diagram and an 'Insert fault' dialog box. The dialog box has options for 'Open fault' (Random, Stuck-at 1, Stuck-at 0, Random) and 'Short fault' (Wired AND, Wired OR, Dominant, Random). It also includes fields for selecting signals and a 'Test-Log-Reset' button.

Applet on basics of test

Introduction into Test and Diagnostics

Circuit selection Working modes Language Help

Working modes

- Setting up testvectors
- Generate testvectors
- Fault simulator
- Guided probing
- Combinatorial fault detection

LFSR

Mode

- BILBO
- CSTP

Configuration

- I1 S1
- I2 S2
- I3 S3
- I4 S4
- I5 S5

Run LFSR

Step

Clear

Manual LFSR

Testvectors Faults Signals Statistics

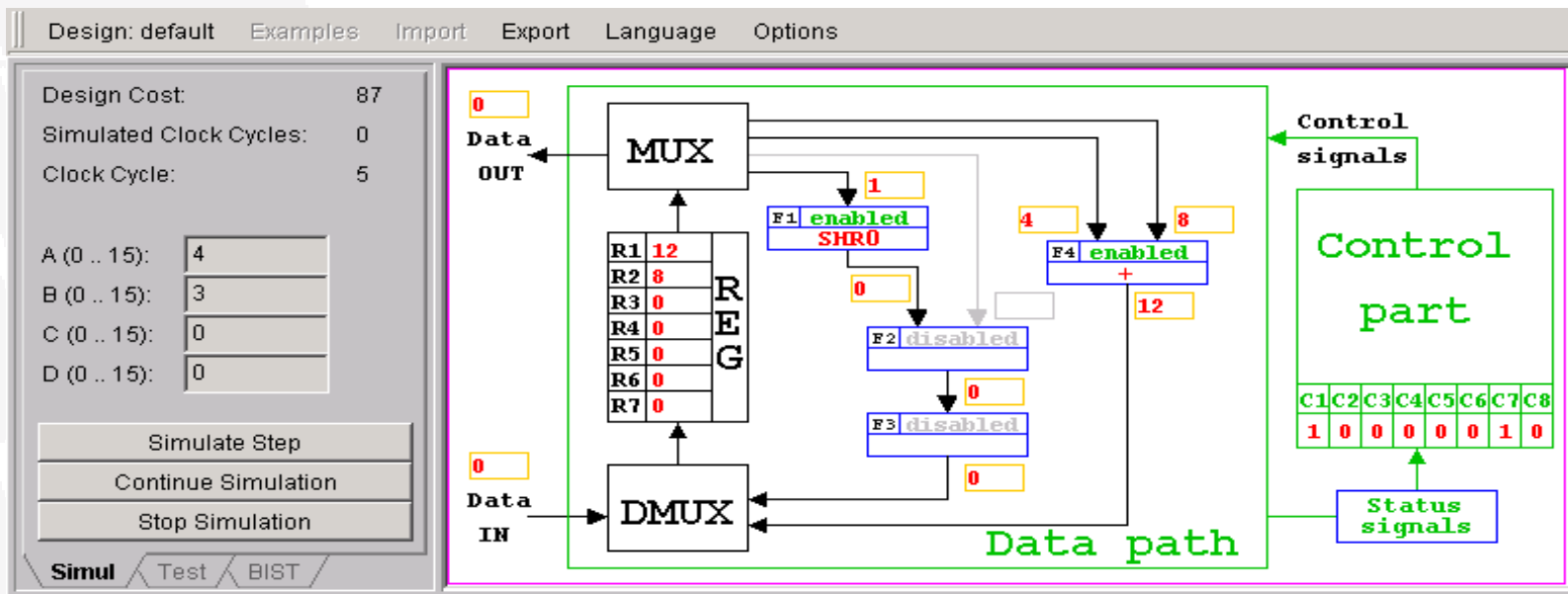
Selected design : ISCAS c17, Mode : Combinatorial fault detection (Counter disabled)

Java Applet Window

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 0 | X | 1 | 0 | 0 | 1 | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 0 | 0 | 0 | X | X | X | 1 | X | 1 | 0 | 0 | 1 | 0 |
| 5 | 1 | X | X | X | 1 | 0 | 0 | X | X | 1 | X | X | X | 0 | 0 |
| 6 | X | X | X | 1 | X | 0 | 0 | X | X | 1 | X | X | X | 0 | 0 |
| 7 | X | X | 1 | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 |

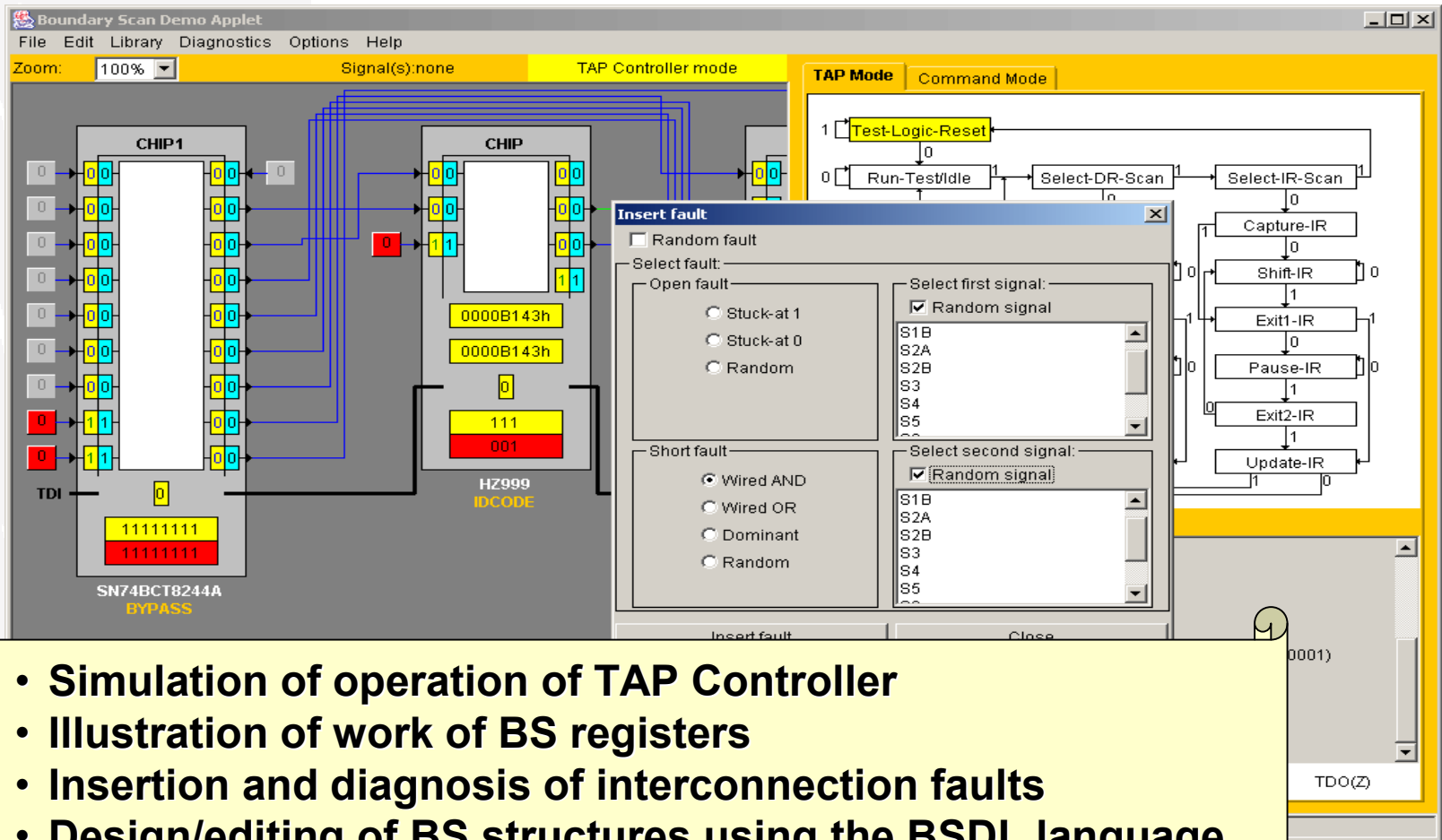
- manual test pattern generation assisted by the applet
- generation of pseudo-random test vectors by LFSR
- fault simulation & study of fault table
- combinational fault diagnosis using fault tables
- sequential fault diagnosis by guided probing

Applet on RT-level design and test



- design of a data path and control path (microprogram) on RT level
- investigation of tradeoffs between speed of the system & HW cost
- RT-level simulation and validation
- gate-level deterministic test generation and functional testing
- fault simulation
- logic and circular BIST, functional BIST, etc.
- design for testability

Applet on Boundary Scan



- **Simulation of operation of TAP Controller**
- **Illustration of work of BS registers**
- **Insertion and diagnosis of interconnection faults**
- **Design/editing of BS structures using the BSDL language**
- **Design/description of the target board using several chips**

Schematic and DD editor

Main functions of the applet are:

- gate-level schematic editor
- SSBDD editor
- schematic ↔ SSBDD on-the-fly converter
- different format reader/converter

Design for Testability

An applet targeted at binding all the applets and the Turbo Tester

AGM, GIF

Applet on Basics of Test & Diagnostics

AGM, DWG

Schematic & DD Editor

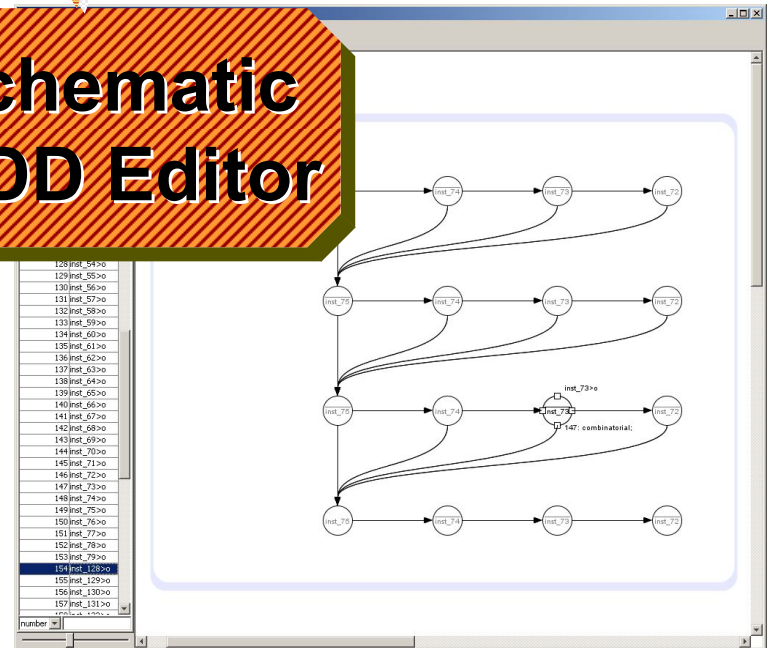
Applet on RTL Design and Test

AGM, GIF

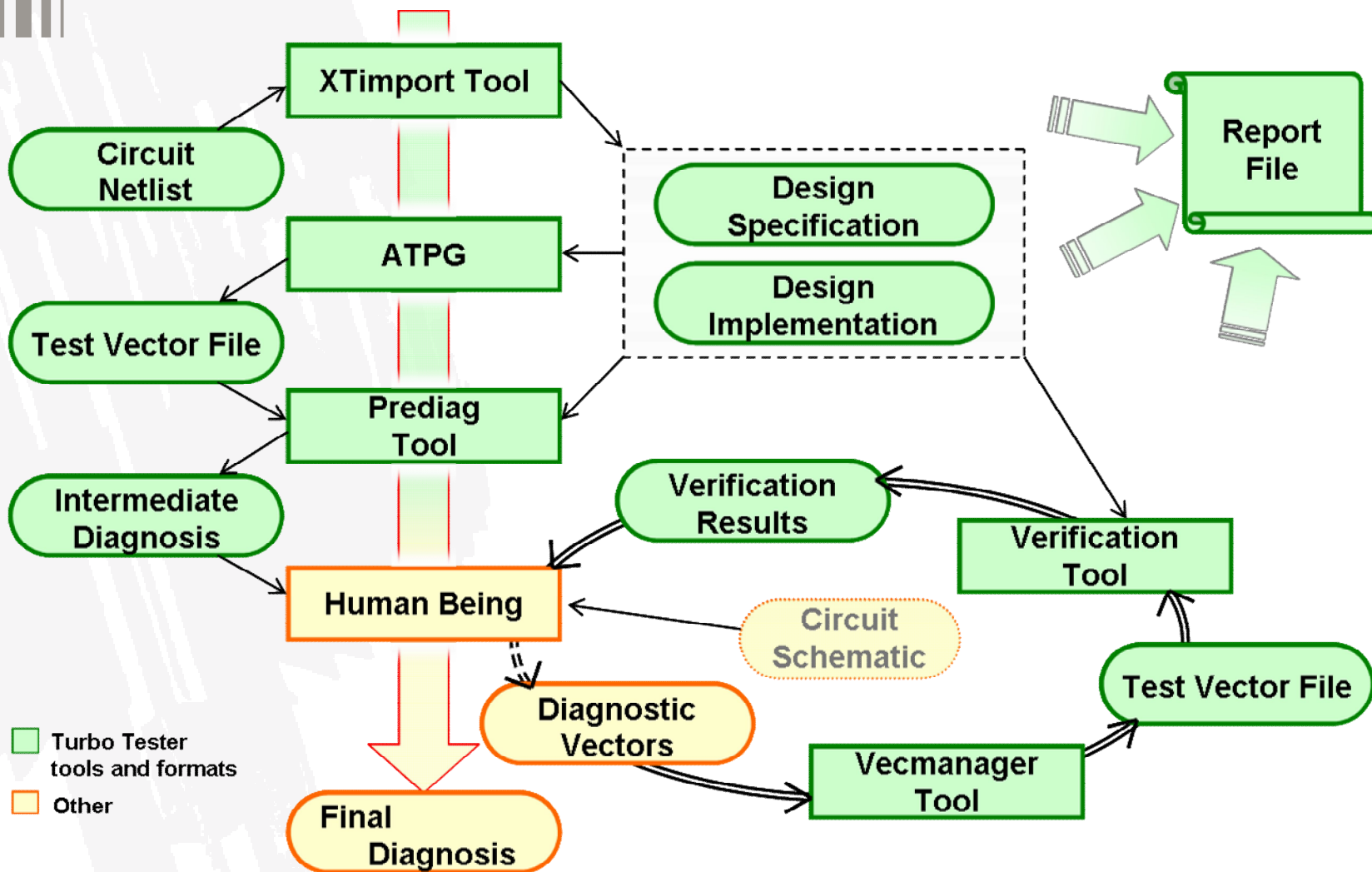
AGM

Applet on Boundary Scan Standard

It is still a work in progress!



Example of a lab work scenario





Conclusions & Discussion

The main features of the platform:

- Research engine + training software
- Layered structure
- HW and SW components
- Remote access
- Distance learning and e-learning
- Computer-aided teaching
- Freeware



Our Tools on the Web

The Turbo Tester home page

<http://www.pld.ttu.ee/tt/>

The Turbo Tester web-server page

<http://www.pld.ttu.ee/webtt/>

DefSim web-server page

<http://www.defsim.com>

Java applets home page

<http://www.pld.ttu.ee/applets/>