Slide 1

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Design for testability and fault tolerance
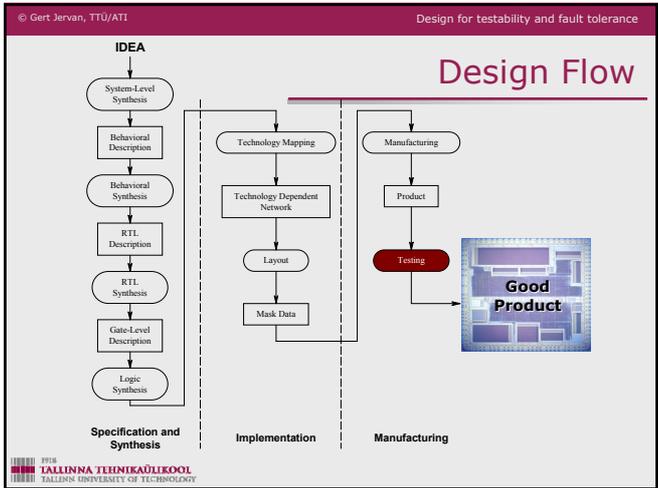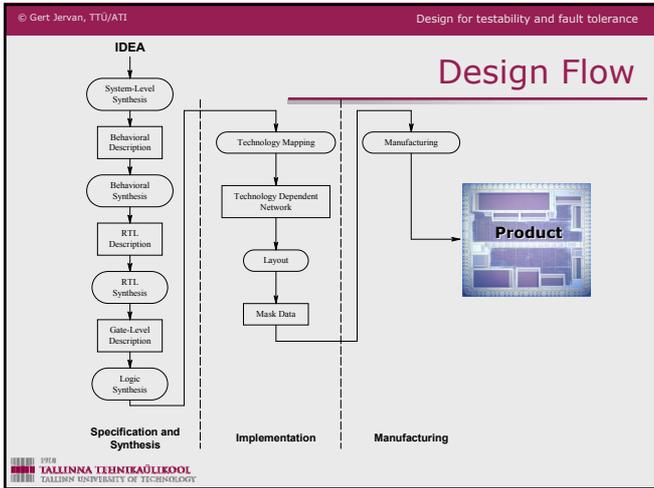
Gert Jervan

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Department of Computer Engineering
Estonia

Slide 2

Overview

✓ Design for testability
  - Built-in self-test (BIST)

✓ Design and technology trends

✓ Fault tolerance
  - System-level fault tolerance

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Slide 3

Design Flow

IDEA

System-Level Synthesis
Behavioral Description
Behavioral Synthesis
RTL Description
RTL Synthesis
Gate-Level Description
Logic Synthesis

Technology Mapping
Technology Dependent Network
Layout
Mask Data

Manufacturing

Product

Specification and Synthesis | Implementation | Manufacturing

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Slide 4

Design Flow

IDEA

System-Level Synthesis
Behavioral Description
Behavioral Synthesis
RTL Description
RTL Synthesis
Gate-Level Description
Logic Synthesis

Technology Mapping
Technology Dependent Network
Layout
Mask Data

Manufacturing
Product
Testing

Good Product

Specification and Synthesis | Implementation | Manufacturing

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Testing

✓ Post-manufacturing
  - Manufacturing defects:
    - stuck-at, bridges, cross-talk, ...
  - Assembly defects:
    - Misaligned components, wrong components, connections, wiring, ...
✓ Operation & maintenance
  - Aging (wearout), radiation (particles), ...

ESD Damage

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84000 RFIC Series

Yes
No/diagnosis

Test Application

Response

Stimuli

© Agilent Technologies

Support from
Automatic Test Equipment

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External Testing

✓ Drawbacks
  - ATE are expensive (typically several million US$)
  - ATE will become more and more inefficient
  - Slow test throughput with long scan chains, especially for core-based designs
  - External Test Data Volume can be extremely high (function of chip complexity)

External Test

Super Tester

Pattern Generation
Precision Timing
Diagnostics
Power Management
Test Control

Very high pin count
Deep memory
Slow throughput

Memory · | Logic · | Mixed-Signal | I/Os & Interconnects

Built-in Self-Test (BIST)

✓ Solution: Dedicated Built-In H/W for embedded test functions
✓ Repartition tester into embedded test and external test functions
✓ Include low H/W cost and high data volume embedded test

External Test

Standard Digital Tester

Limited Speed/ Accuracy

Low Cost-per-Pin

Embedded Test (Built-in)

Pattern Generation
Result Compression
Precision Timing
Diagnostics
Power Management
Test Control

Support for
Board-level Test
System-Level Test

Memory · | Logic · | Mixed-Signal | I/Os & Interconnects

Chip, Board or System

Problems with BIST

Progressive Coverage of Test Patterns

✓ Typical test generator: Linear Feedback Shift Register (LFSR)
  - LFSR generated vectors are pseudorandom by their nature
✓ Pseudorandom vectors:
  - Very long test application time
  - Not guaranteed high fault coverage

BIST Improvement

Possible solution:

Combination of **pseudorandom** test and **deterministic** test to form a **Hybrid BIST** solution in order to:
  - increase the fault coverage
  - reduce the test cost

Fault Coverage / Time

Hybrid BIST – System Level Test Architecture

Embedded Tester — Test Controller — Tester Memory

C2670 | BIST
C3540 | BIST
Test access mechanism
BIST C1908 | BIST C880 | BIST C1355

SoC

Hybrid BIST – The Concept

Amount of Stored Patterns

FC

ATPG

PRG

Max. fault coverage

Time (1) | Time (2) | Time (3)

Different Approaches

Slide 1

Cost Calculation for Hybrid BIST

Total Cost C_{TOTAL}

Cost of pseudorandom test patterns C_{GEN}

Cost of stored test C_{MEM}

Number of remaining faults after applying k pseudorandom test patterns $r_{NOT}(k)$

Number of pseudorandom test patterns applied, k

$$C_{TOTAL} = C_{GEN} + C_{MEM} = \alpha L + \beta S$$

Slide 2
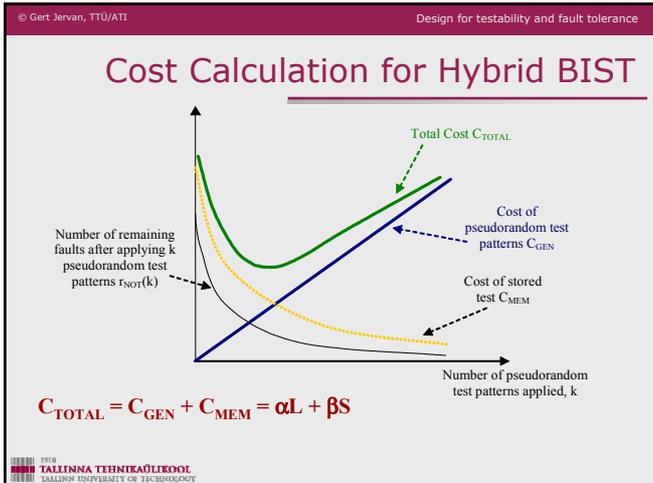
Our Contributions

- ✓ Developed fast estimation method for various optimization calculations
- ✓ Proposed algorithms for finding the shortest test length under given memory constraints
  - Single core and multicore systems
  - Serial and parallel (broadcasting) test architectures
- ✓ Proposed algorithms for test cost minimization
- ✓ Proposed algorithms for test energy minimization
- ✓ Proposed algorithms for test time minimization and test power control in the abort-on-first-fail environment

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Today and future

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Slide 4

Technology Trends

Drawn to the same scale

90nm MOS Transistor

1.0 µm
Mid 1980s
Speed: 10 MHz

0.1 µm
Early 2000's
Speed: 3 GHz

Today: 65 nm, going down to 22 nm by 2016

Slide 5
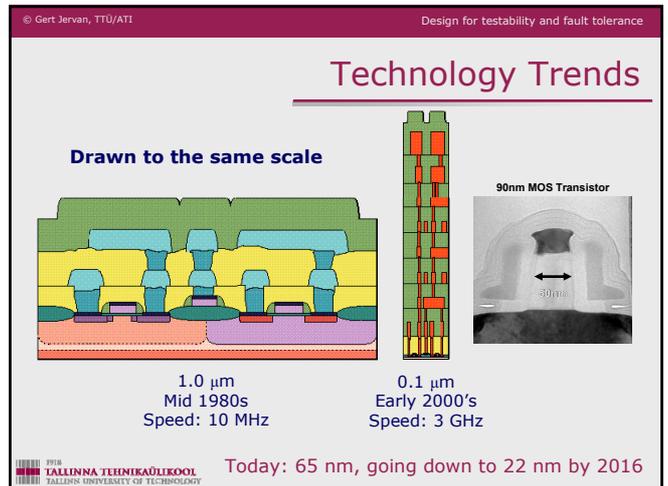
Benefits of Technology Scaling

- ✓ Benefits of scaling the dimensions by 30%:
  - Reduce gate delay by 30% (increase operating frequency by 43%)
  - Double transistor density
  - Reduce energy per transition by 65% (50% power savings @43% increase in frequency)

Slide 6
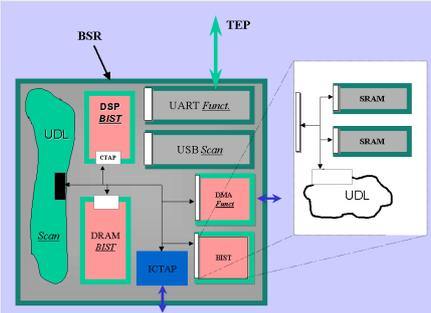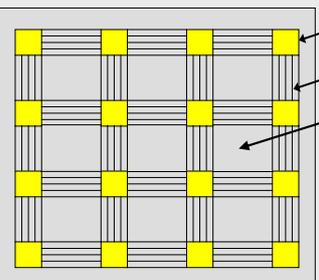
The Evolution of Systems

Algorithm on a Chip
- Hardwired Computation
- Hardwired Communication

System on a Chip
- Programmable Computation
- Hardwired Communication

Network on a Chip
- Programmable Computation
- Programmable Communication

Algorithm on a Chip

The Evolution of Systems

| Algorithm on a Chip | Hardwired Computation |
| | Hardwired Communication |

| System on a Chip | Programmable Computation |
| | Hardwired Communication |

| Network on a Chip | Programmable Computation |
| | Programmable Communication |

Design Trends

✓ System on a Chip (SoC)

The Evolution of Systems

| Algorithm on a Chip | Hardwired Computation |
| | Hardwired Communication |

| System on a Chip | Programmable Computation |
| | Hardwired Communication |

| Network on a Chip | Programmable Computation |
| | Programmable Communication |

Network on a Chip

Switch

Wires

Resources

Computational
RF / Analog
Processor cores
Hardware blocks
FPGAs

Storage

NoC Example
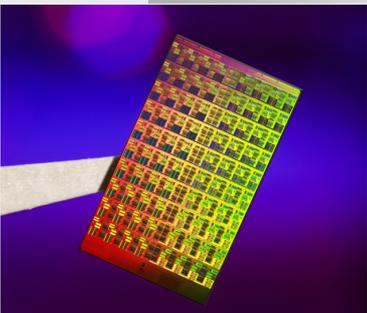
Intel 80 core teraflops research chip

Implications to Design

- ✓ Design fabric will be Regular
- ✓ Will look like sea-of-transistors interconnected with regular interconnect fabric
- ✓ Shift in the design efficiency metric
  - From Transistor Density to Balanced Design

BUT

- ✓ Manufacturing of these sub-nanometer chips defect-free is almost impossible (yield is below acceptable levels)
- ✓ Increasing importance of transient and intermittent faults (due to the environment)

Transient faults

- ■ Happen for a short time
- ■ **Corruptions of data, miscalculation in logic**
- ■ Do not cause a permanent damage of circuits
- ■ Causes are outside system boundaries

Radiation
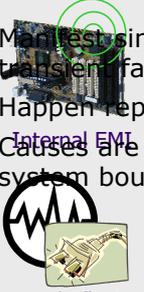
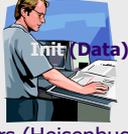Electromagnetic interference (EMI)

Lightning storms

Intermittent faults

- ■ Manifest similar as transient faults
- ■ Happen repeatedly
- ■ Causes are inside system boundaries

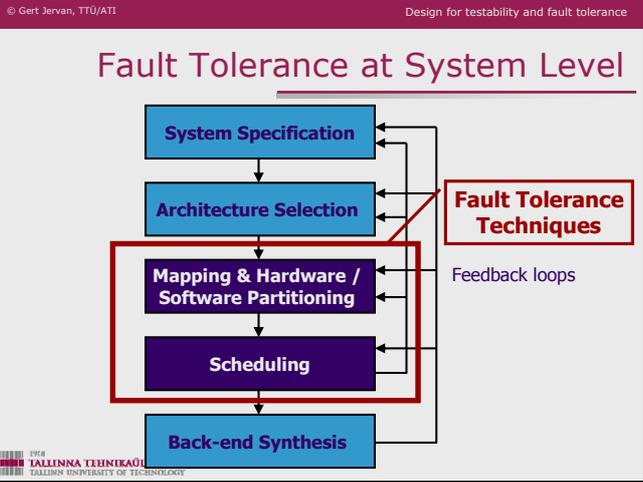Internal EMI

Crosstalk

Init(Data)

Power supply fluctuations

Software errors (Heisenbugs)

Fault Tolerance

- ✓ Fault tolerance and reliability are system issues, requiring work with hardware, software, time and information
- ✓ It is incrasingly hard to work with hardware issues
- ✓ More work will be done at the system level
  - ■ Built-in self-repair
    - • Dynamic reconfiguration
    - • Re-execution, replication, checkpointing, ...
    - • Task remapping/rescheduling

Fault Tolerance at System Level

- System Specification
- Architecture Selection
- Mapping & Hardware / Software Partitioning
- Scheduling
- Back-end Synthesis

Fault Tolerance Techniques

Feedback loops

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The problem to be solved:

How to design reliable system out of non-reliable hardware?

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